DAMAGE PROFILES IN SILICON and THEIR IMPACT ON DEVICE RELIABILITY, Part II

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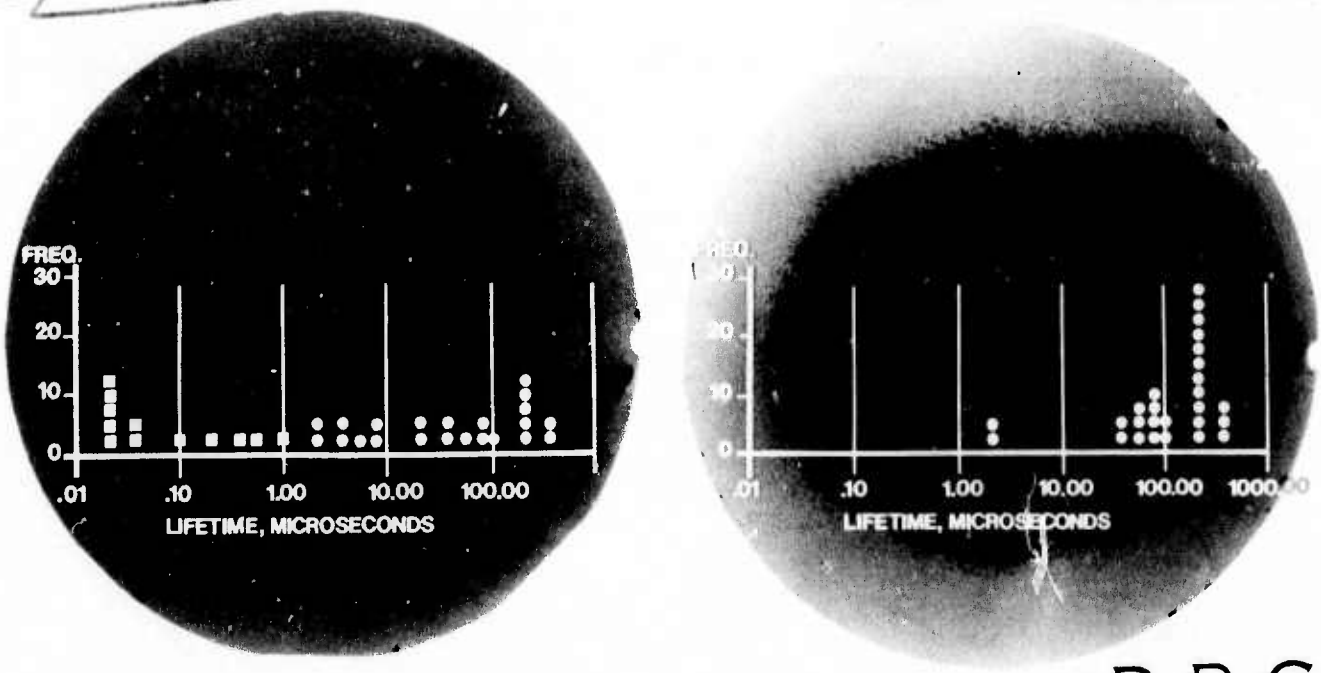

Lifetime improvement in silicon through ISS. (Left) Lifetime distribution in standard wafer. (Right) Lifetime distribution after ISS. (See Chapter 2)

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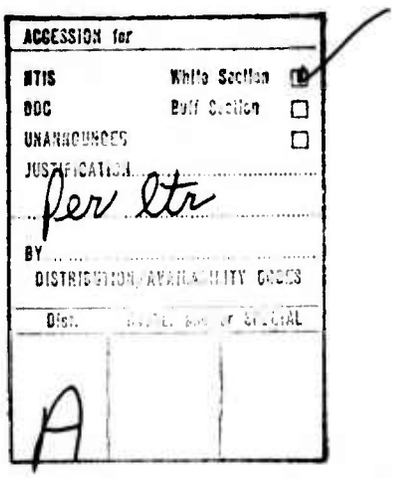


SUMMARY

The report consists of two chapters. Chapter 1 discusses experimental and theoretical investigations of the growth kinetics of oxidation induced stacking faults. Experimentally it is found that stacking fault growth during wet or dry oxidation follows the equation: $l = A_o t^{0.77} \times \exp(-\Delta H_f / kT)$ where l is the stacking fault length, t is the oxidation time, A_o is equal to $(1.38 \pm 0.06) .10^9$ for wet oxidation and equal to $(9.5 \pm 0.5) .10^8$ for dry oxidation, and $\Delta H_f = 2.2$ eV the activation energy for fault formation. Theoretically, it is shown that growth of stacking faults can be described through condensation of silicon interstitials at the fault site during oxidation. Condensation of silicon interstitials is controlled through a tensile stress in the silicon surface generated during the formation of the SiO_2 film on the silicon surface. Good agreement between experimental and calculated data for fault length and activation energy is obtained.

Chapter 2 discusses the technique of Impact Sound Stressing (ISS). ISS is applied (a) to produce damage on silicon surfaces in a controlled manner and (b) to achieve "damage gettering" in silicon. ISS damage introduced on the wafer backside is used to monitor generation-lifetime of electrical carriers during semiconductor processing. This is shown for

silicon substrates, for epitaxial silicon films, and for epitaxial silicon films grown on ion-implanted surfaces. ISS improves lifetime in silicon by several orders of magnitude. Such lifetime improvements on ISS'ed silicon wafers are correlated with a reduction of crystallographic defects. A quantitative relation between lifetime and defect density is given.

Chapter 1

GROWTH KINETICS OF STACKING FAULTS IN OXIDIZED SILICON

by

K. Yang, G. H. Schwuttke, and H. Kappert

1. INTRODUCTION

In semiconductor manufacturing the generation of defects in silicon wafers during device processing is an area of major concern. Numerous investigators are active in this field and have well documented that the combination of crystal defects and impurity precipitation encountered during device processing can alter electrical properties of silicon such as wafer conductivity, carrier mobility, and minority carrier lifetime. As a result of these changes defects in silicon wafers are the cause of increased leakage currents in devices and have a negative influence on processing yield in the fabrication of integrated circuits.

One of the fundamental processes in silicon semiconductor manufacturing is oxidation. Oxidation of silicon at high temperatures is known to generate stacking faults in the surface layer of the wafer. These faults are readily observed by surface etching and optical microscopy, by x-ray topographic techniques, or by transmission electron microscopy.

Numerous papers have already been published on the subject of nucleation and growth of oxidation induced stacking faults in

silicon. The fact that so many papers have been published[1-14] is evidence that nucleation and growth of oxidation-induced stacking faults in silicon is a very complex problem which even today is not completely understood. Published papers on the growth kinetics of such faults show considerable disagreement.[1-4] Queisser and vanLoon[1,2] observed that the fault length (l) is proportional to oxidation time (t), for steam oxidation, and to $t^{0.8}$ to $t^{0.9}$ for wet oxidation. Fisher and Amick [3] reported that $l = ct^{0.8} + d$, where c and d are experimental constants. On the other hand, Mayer [4] found that fault growth is determined by a parabolic law. The activation energy for the formation of stacking faults, ΔH_f, also differs greatly according to these authors, and ranges from 0.25 to 2 eV. [1-4]

Booker and Tunstall[5] demonstrated through detailed electron microscopy work that such faults are extrinsic stacking faults bounded by Frank partial dislocations (see also Chapter 2, Part I of this report). The crystallographic nature of these faults was also investigated by several other investigators.[6-8] Based on this work it is generally accepted that fault growth is associated with the climb of Frank partials from the surface into the silicon substrate, and that the growth mechanism is related to the absorption or emission of point defects by diffusion. Such a growth mechanism has been proposed by several investigators. [5-12] However, no quantitative relationship has yet been published to describe

the dependence of fault growth on oxidation time and temperature.

A recent paper by Hu [13] presents a model that postulates surface regrowth at the Si-SiO_2 interface due to excess interstitials. His model predicts quantitatively the parabolic growth of stacking faults with an activation energy ΔH_f equal to one half of the activation energy for the parabolic growth oxide. However, Hu's predictions do not agree too well with most of the experimental data published on growth kinetics.[1-3,6]

It appears that major difficulties encountered in the study of this problem relate to the nucleation as well as the growth of oxidation induced stacking faults.

In Chapter 2 of ARPA Report 7, Part I, we have addressed the nucleation of stacking faults and have shown that high stress concentrations due to dislocation pile-ups may cause microsplits of 1000Å or smaller which can nucleate stacking faults during dry oxidation.

This chapter reports experimental results and some new ideas on the growth of such faults during oxidation. It investigates the growth kinetics for wet and dry oxidation and presents a growth model which is in good agreement with the experimental results.

2. EXPERIMENTAL APPROACH

Silicon wafers of <100> orientation grown by the Czochralski technique and boron-doped to a resistivity of 2 Ω-cm were used for this study. The wafers were subjected to a chemical polish to remove all visible surface damage. No intentional damage was applied to wafer surfaces prior to oxidation.

The wafers, three for each run, were oxidized immediately after cleaning in an oxidation furnace which controlled the desired temperature within $\pm 2°C$. After oxidation, the oxide thickness was measured by ultraviolet interferometry. Subsequently the oxide was removed through a hydrofluoric acid dip.

The wafers were Sirtl etched to reveal stacking faults. The fault density on each wafer varied from $\sim$ 100 to 10^4 per cm^2. The faults were found to be about equal in size, independent of fault density, on each wafer. The fault length, as reported in this paper, is the average value of at least 20 measured faults on each wafer. The standard deviation for the fault length reported is better than 3%.

3. RESULTS. EXPERIMENTAL AND THEORETICAL

3.1 Growth Kinetics of Stacking Faults

In Fig. 1 the length of stacking faults, l, is plotted as a function of oxidation time, t, for wet and dry oxidation. The relationship shown in Eq. (1) has been determined from this plot:

$$l = At^{0.77} \tag{1}$$

In Eq. (1) the length l is expressed in μm, the time t in hours, and A is an experimental constant. This relationship holds for both wet and dry oxidation at different temperatures. However, stacking faults obtained through a wet oxidation are longer than those grown by a dry oxidation.

The activation energy for the fault formation, ΔH_f, can be measured from a plot of log l vs 1/T as given in Fig. 2. Accordingly, the activation energy, ΔH_f, is 2.2 eV, nearly independent of wet and dry oxidation conditions. Differences in activiation energy are found for wet and dry oxidation for temperatures below 1050°C. At these temperatures, ΔH_f for dry oxidations seems to increase while the oxidation temperature decreases.

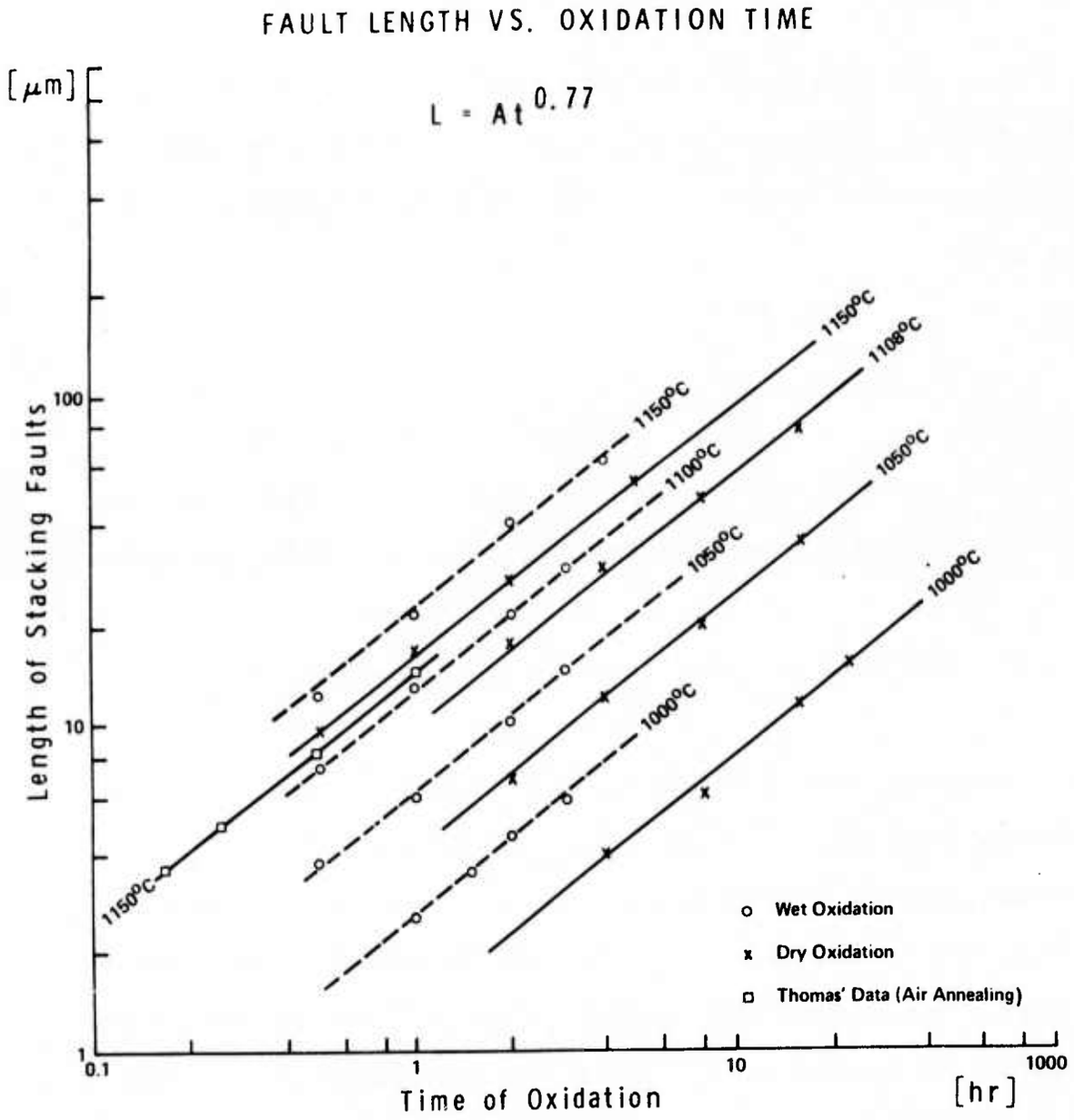


Fig. 1. The effect of oxidation time on the fault length.

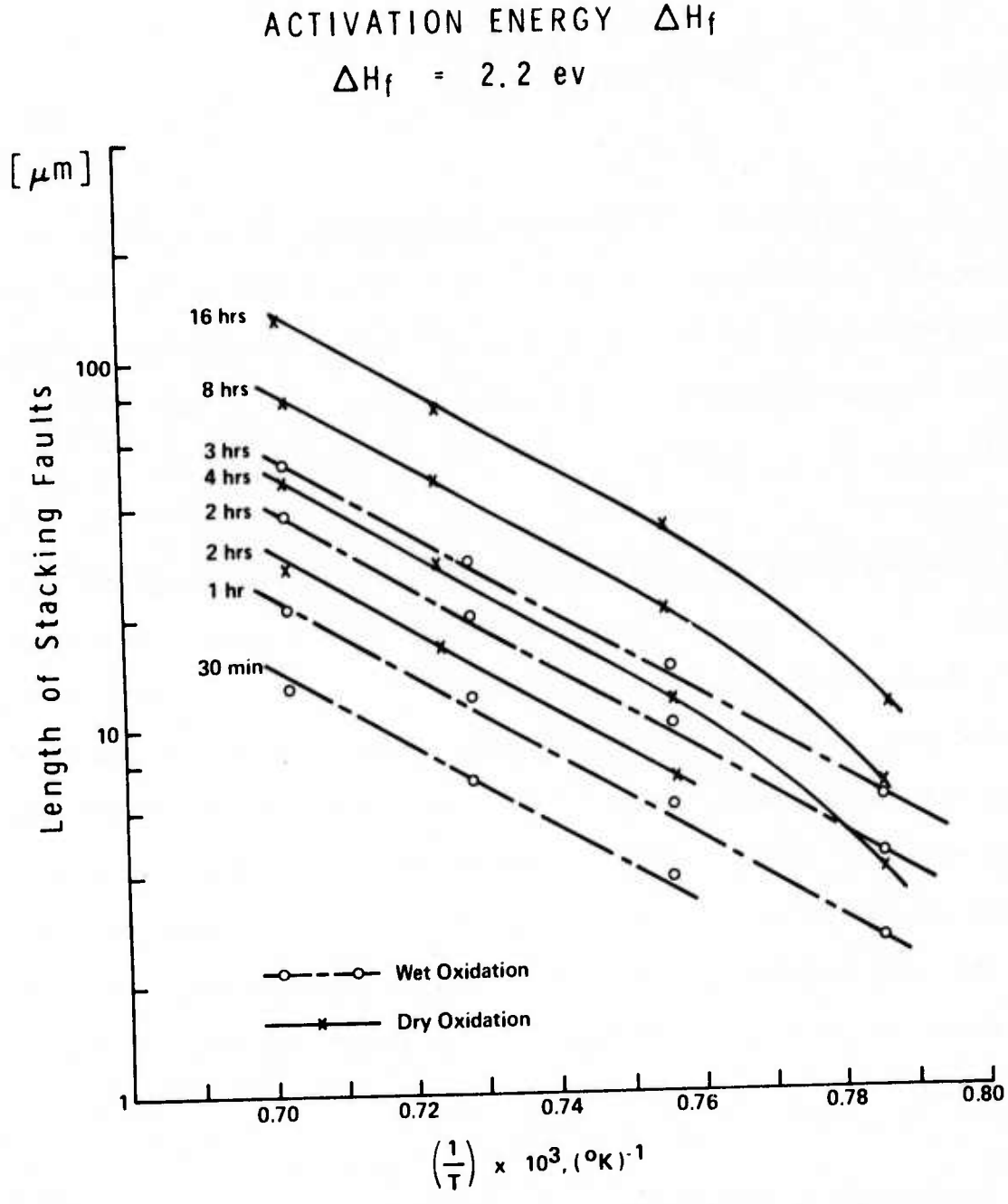


Fig. 2. The effect of oxidation temperature on the fault length.

The relationship of Eq. (1) can be expressed in simple Arrhenius form as shown in Eq. (2).

$$l = A_o t^{0.77} \cdot \exp\left[-\frac{\Delta H_f}{kT}\right] \qquad (2)$$

A_o is an experimental constant independent of oxidation temperature. The value of A_o is $(1.38 \pm 0.06) \times 10^9$ for wet oxidation, and is $(9.5 \pm 0.5) \times 10^8$ for dry oxidation. For the same oxidation time and temperature, the length ratio of $(l)_{wet}/(l)_{dry}$ is $(A_o)_{wet}/(A_o)_{dry} = 1.46 \pm 0.16$.

A comparison of our data with published values is given in Table 1. Our results are in good agreement with those obtained by Fisher and Amick [3] and Thomas [14]. A set of Thomas' data, also obtained from wafers of <001> orientation, is plotted in Fig. 1 for comparison. The relatively shorter fault length observed by Thomas may be a result of air annealing instead of dry oxidation used in our experiment. It is interesting to note that the activation energy for fault shrinkage in vacuum annealing, 2.1 ± 0.2 eV (Ref. 6) is about the same as for fault growth.

3.2 Oxidation Parameters

A plot of oxide thickness as a function of oxidation time is shown in Fig. 3. Accordingly, the oxide growth follows a

Table 1. Kinetic data for the growth of stacking faults

Ref.	Substrates	Resistiv. Ω-cm	Oxidation	Relation	ΔH_f, [eV]
1&2	N(100) P(100)	0.07 0.04	Steam Wet	$l \propto t$ $l \propto t^{0.8 \sim 0.9}$	0.25 1.6
3	N(111) N(110) P(111)	0.01&1 11 15 15	Steam	$l=ct^{0.8}+d$	2
4	N(100) P(100)	1-10 1-15	Steam & Dry	$l \propto t^{0.5}$	
Present Data	P(100)	2	Wet & Dry	$l=At^{0.77}$	2.2

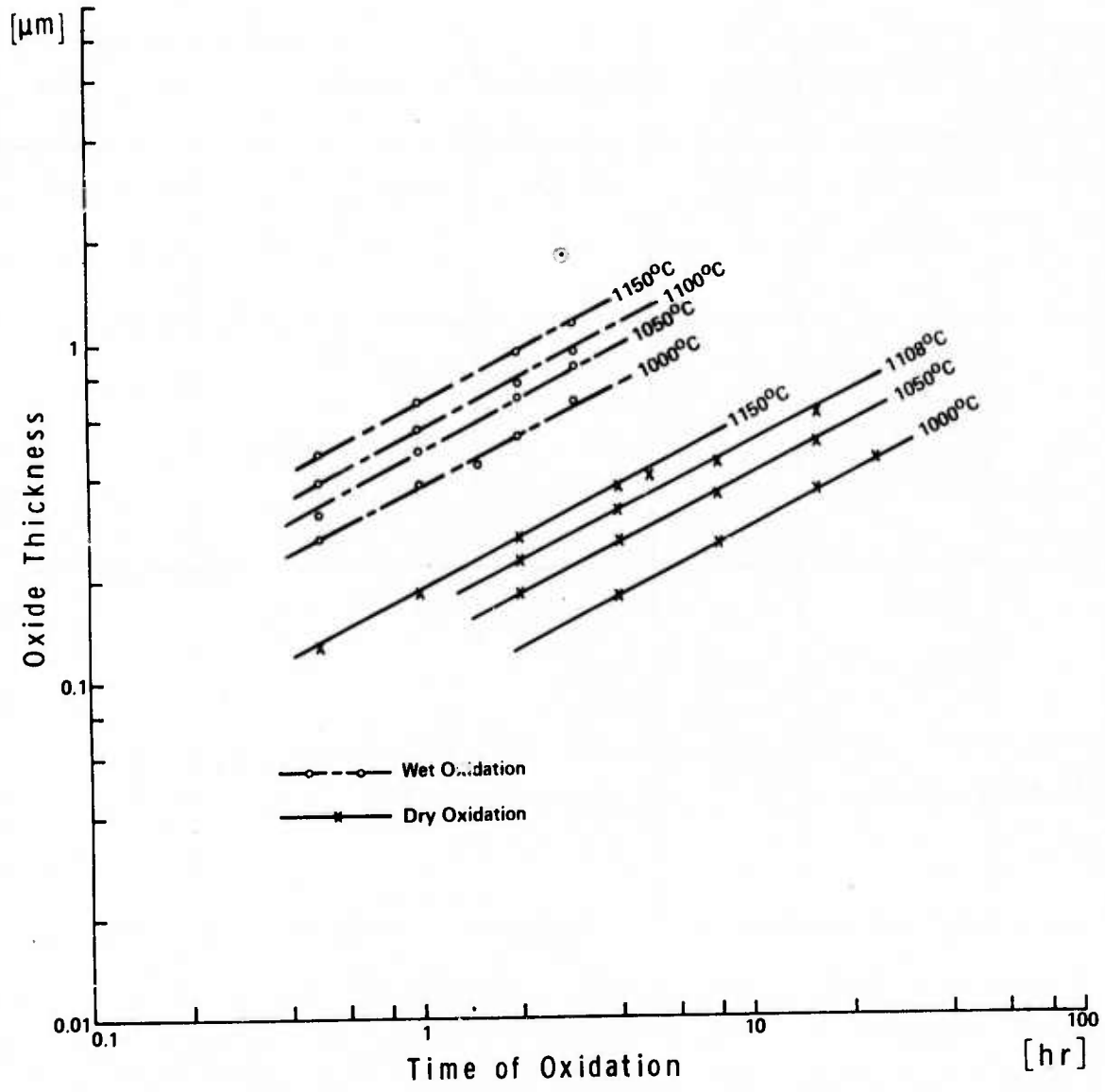


Fig. 3. The effect of oxidation time on the oxide thickness.

parabolic relationship in the temperature range shown. Therefore it can be assumed that the oxidation rate is diffusion controlled [15]. Equation (3) follows from the plot of Fig. 3

$$X = (Bt)^{0.5} \tag{3}$$

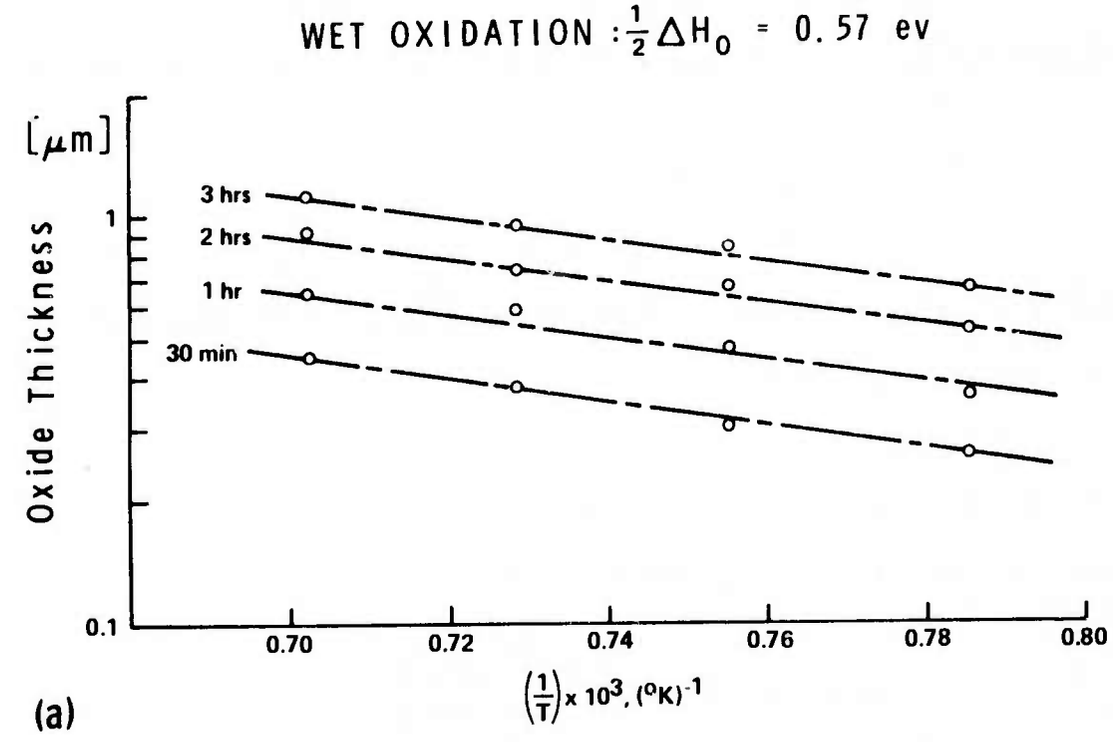
where x is the oxide thickness in μm and B is the parabolic rate constant in $\mu m^2/hr$.

As shown in Fig. 4, the oxide growth can be expressed by the simple Arrhenius relationship given in Eq. (4):

$$X = (B_o t)^{0.5} \exp\left[-\frac{\Delta H_o}{2kT}\right] \tag{4}$$

Where ΔH_o is the activation energy for oxide growth in the diffusion-controlled region. For dry oxidation the value of ΔH_o is 1.28 eV and for wet oxidation it is 1.14 eV. These values are in good agreement with those reported by Thurston [16], but are slightly higher than those obtained by Deal [15] for wet oxidation. The value of $(B_o)^{1/2}$ is 67.5 $\pm$ 0.8 μm/hr for wet oxidation, and is 33.0 $\pm$ 1.0 μm/hr for dry oxidation.

These results indicate that the growth of stacking faults as well as the growth of oxide is strongly related to the oxidation conditions, such as ambiance, time, and temperature.



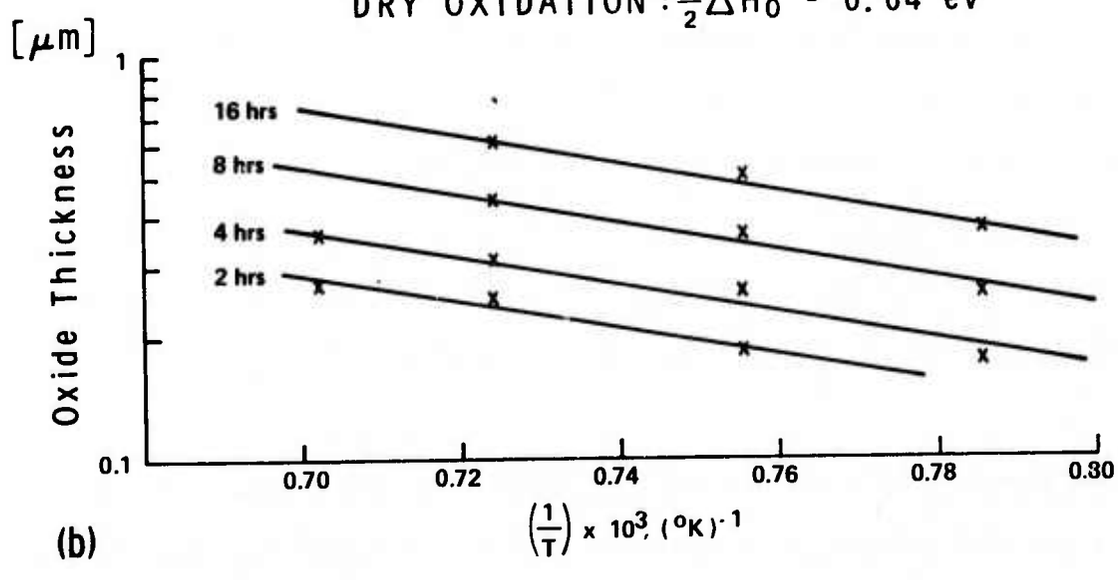


Fig. 4. The effect of oxidation temperature on the oxide thickness for wet (a) and dry (b) oxidation.

3.3 Effect of Oxide Thickness

The effect of oxide thickness on fault growth was further investigated. Several wafers with different oxide thicknesses were cleaved into two halves after the first oxidation. The oxide on the first half was removed with HF, while on the second half, the oxide was retained on the surface. These half wafers were subjected a second time to the same oxidation (wet, 1100°C, 1 hr).

The following results were obtained for the fault length. In wafer half 1 (oxide removed) the fault length obtained after the second oxidation was essentially the same as the fault length obtained through a single oxidation equal in time to the two separate oxidations. This indicates that growth of these faults continued at the same rate during the second oxidation. In wafer half 2 (oxide retained) the fault length found after the second oxidation showed an oxide thickness dependence such that the fault length decreased with the oxide thickness (Table 2). A similar trend is reported in Ref. 3.

3.4 Stacking Fault Growth Model

In this model, we conceive that after fault nucleation at sites of mechanical damage (see Chapter 2, ARPA Report 7,

Part I) (and/or at impurity precipitates) stacking faults grow by the following mechanism:

- The growth of stacking faults occurs through climb of Frank partial dislocations. The climb is assisted by the stress generated in silicon and exerted by the SiO_2 film.

- Under the action of this stress, an undersaturation of interstitials occurs near the partial dislocation and is in quasi-equilibrium with the interstitial concentration at the Si-SiO_2 interface.

- The partial dislocation surrounding the fault acts as a sink for interstitials. The growth of stacking faults is controlled by the absorption of interstitials provided for by a diffusive flow of interstitials to the sink.

This model accepts the importance of stress buildup at the oxidized surface for the growth of stacking faults. The influence of stress on stacking fault growth is well established[1-3,14,17].

The exact mechanism of self-diffusion in silicon is still a subject of active research[18,19]. In our model, self-diffusion in silicon follows the interstitialcy mechanism of Seeger and Chik[18].

A quantitative description of our model is given in the appendix of this chapter. Accordingly, the dependency of stacking fault growth on oxidation time and temperature is as follows:

$$l = A_o\, t^{0.75} \exp\left[-\frac{Q_{SD} + 0.5\,\Delta H_o}{2kT}\right] \qquad \text{(A14)}$$

$$A_o = 4\left[\frac{V_i \cdot D_o \cdot K \cdot B_o^{1/2}}{1.5\ kT}\right]^{1/2} \qquad \text{(A15)}$$

4. Discussion

In general we find that our model of stacking fault growth gives results in good agreement with the experiment. This is shown in the following:

Equations (A14) and (A15) indicate that growth of stacking faults is proportional to $t^{0.75}$. This agrees well with the experimental result [see Eq. (1) and Fig. 1].

Note also that for oxidation carried out in the "reaction controlled" region[15] the exponent 0.75 approaches 1 and thus fault growth becomes proportional to time. Linear stacking fault growth with time has been observed previously.[6]

The activation energy for fault formation is: $\Delta H_f = 0.5(Q_{SD} + 0.5\Delta H_o)$. Calculated values for ΔH_f range from 2.72 to 2.86 eV for wet oxidations and from 2.75 to 2.89 eV

for dry oxidations. Experimentally we find 2.2 eV (Fig. 2) a value much smaller than calculated for wet and dry oxidation. Values for Q_{SD} as listed in the literature range from 4.86 to 5.14 eV.[20,21]

The discrepancy between calculated and measured values for ΔH_f can be reduced if we consider that self-diffusion in the vicinity of stacking faults may be significantly larger as compared to its value in the bulk. In low-stacking-fault energy materials, such an enhancement leads to pipe diffusion and can be expected to be appreciable. Pipe diffusion lowers Q_{SD} by an amount of 1/4 Q_{SD}.[22,23] Accordingly, the calculated value of ΔH_f becomes 2.1 to 2.2 eV, in good agreement with our experimental value of 2.2 eV.

The ratio of fault length induced in wet and dry oxidation can be predicted from $(A_o)_{wet}/(A_o)_{dry}$. For identical oxidation time and temperature, this ratio is

$$\frac{(\ell)_{wet}}{(\ell)_{dry}} = \frac{(A_o)_{wet}}{(A_o)_{dry}} = \frac{(B_o)^{1/4}_{wet}}{(B_o)^{1/4}_{dry}} = 1.43 \pm 0.004$$

This also compares well with the experimental value of 1.46 $\pm$ 0.16 (see page 6).

Equation (A14) indicates that fault growth is independent of the angle, θ, between the (111) planes and the wafer surface. For <110> oriented wafers, Fisher and Amick [3] observed that

stacking faults grow preferentially in the (111) planes that intersect the surface with an angle of 90° rather than that with 35.3°. Prussin [11], however, did not observe such an angular dependency. He attributed the defects observed in the shallow intersecting planes to dislocation loops as judged from the appearance of Sirtl etched surfaces. However, recent electron microscopic examinations of such defects indicate that they are stacking faults and not dislocation loops.[5]

Our investigation on < 115 > oriented wafers show that fault growth is independent of θ. An example is given in Fig. 5. For wafers of this orientation, two (111) planes intersect the wafer surface at 38.9° and 70.7° along the $[1\bar{1}0]$ trace, and the other two at 56.6° along the $[\bar{2}\bar{3}1]$ and $[\bar{3}\bar{2}1]$ directions. No significant difference in fault length is observed in Fig. 5.

The proposed model does not explain the results of double oxidation given in Table 2. It actually predicts a longer fault length with a thicker retained oxide and not a shorter one as observed in the experimental results. The reason for this fault "shrinkage" has not become clear during this investigation.

Experimentally it is found that the fault length, l_2, obtained in the second oxidation is related to the initial oxide thickness X_i, and the final oxide thickness X_f according to:

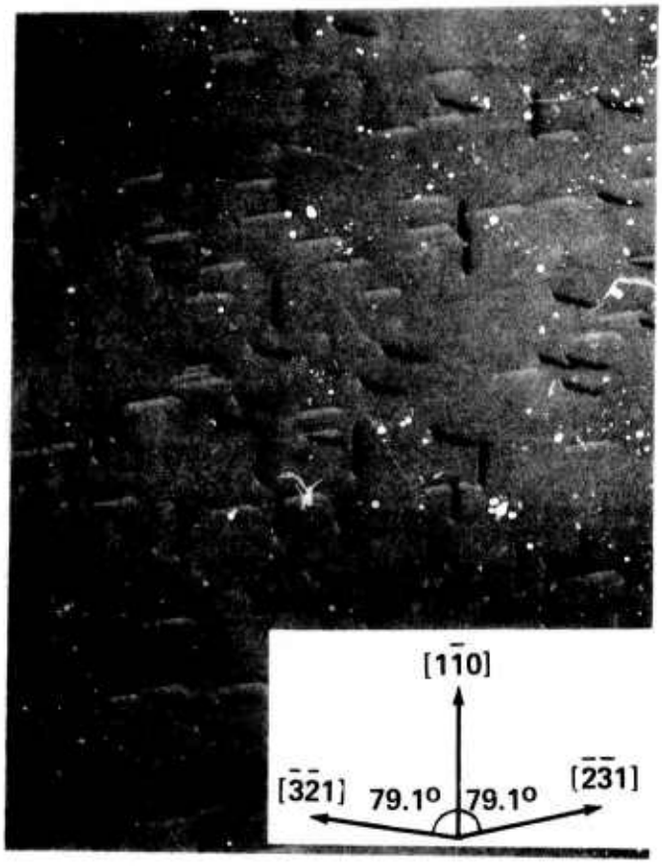


Fig. 5. Stacking faults induced in the surface of a <115> oriented wafer.

Table 2. Effect of oxide thickness on the growth of stacking faults induced in the second oxidation

Sample	1st Oxidation	2nd Oxidation	x_i[μ]	x_f[μ]	l_2[μ]
0	Wet, 1100°C,1 hr		0.55		13.0
1	Wet, 1000°C,0.5hr	Wet,1100°C, 1 hr	0.26	0.61	11.7
2	Wet, 1000°C, 1 hr	"	0.37	0.66	9.9
3	Wet, 1000°C,1.5hr	"	0.45	0.71	9.5
11	Wet, 1100°C, 1 hr	"	0.55	0.77	9.1
5	Wet, 1000°C, 3 hr	"	0.63	0.83	9.1
16	Wet, 1150°C, 1 hr	"	0.66	0.86	8.5
17	Wet, 1150°C, 2 hr	"	0.93	1.08	7.9
18	Wet, 1150°C, 3 hr	"	1.13	1.25	7.6

$$l_2 = A' (X_f^{1.5} - X_i^{1.5}); \; A' = A/(B)^{1/2} \qquad (6)$$

This equation is in agreement with similar results published by other investigators.[6] Using sample No. 0 (Table 2) as a reference point (l_1, X_1), the effect of retained oxide on fault length during the second oxidation is plotted in Fig. 6 using l_2/l_1 vs $(X_f^{1.5} - X_i^{1.5})/X_1^{1.5}$. This suggests that for retention of oxide on the surface, subsequent fault growth during a follow-on oxidation leads to a fault length determined by the net growth of oxide from X_i to X_f in a single oxidation.

5. SUMMARY

Experimental and theoretical investigations of the growth kinetics of oxidation-induced stacking faults are presented. Experimentally it is found that stacking fault growth during wet or dry oxidation follows the equation: $l = A_o t^{0.77} \exp\{-\Delta H_f/kT\}$ where l is the stacking fault length, t is the oxidation time, A_o is equal to $(1.38 \pm 0.06) .10^9$ for wet oxidation and equal to $(9.5 \pm 0.5) .10^8$ for dry oxidation, and $\Delta H_f = 2.2$ eV the activation energy for fault formation. Theoretically, it is shown that growth of stacking faults can be described through condensation of silicon interstitials at the fault site during oxidation. Condensation of silicon interstitials is controlled through a tensile stress in the silicon surface generated during the formation of the SiO_2 film on the silicon surface. Good agreement between experimental and calculated data for fault length and activation energy is obtained.

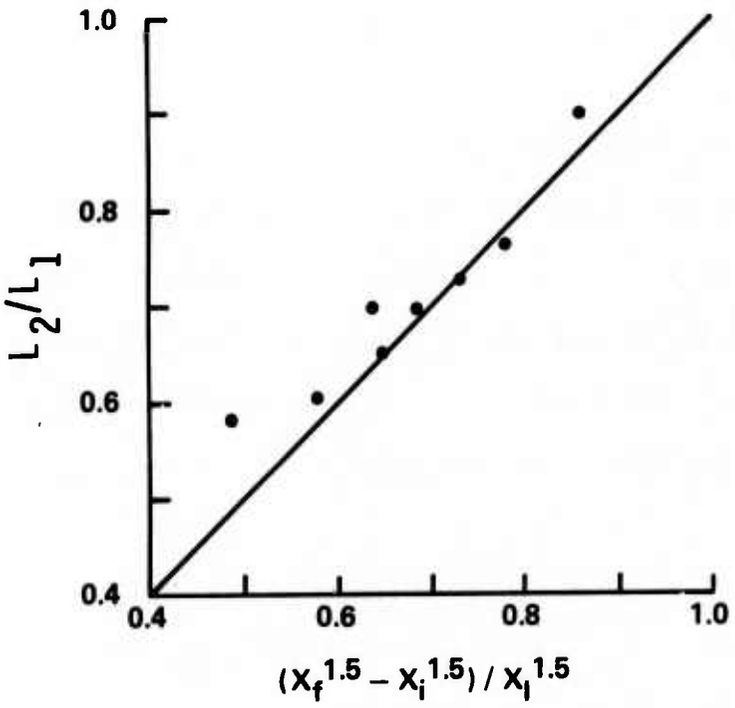


Fig. 6. The effect of retained oxide on the fault length induced in the second oxidation.

6. APPENDIX: GROWTH MODEL THEORY (by K. Yang)

Consider that a fault lying in the $(\bar{1}1\bar{1})$ plane has a shape of a truncated circle, as shown in Fig. 7. During oxidation, silicon is subjected to a maximum tensile stress at the $Si\text{-}SiO_2$ interface according to Ref. 24:

$$\sigma_{xx} = \sigma_{yy} = -4\frac{X}{d}\sigma_o = KX \qquad (A1)$$

where X is the oxide thickness, d is the wafer thickness, σ_o is the stress in the oxide and K as defined is a constant nearly independent of the oxide thickness. Under the action of the resolved normal stress of σ_{yy} in the $(\bar{1}1\bar{1})$ plane, the Frank dislocation of the fault experiences a climb force. The energy change, per interstitial absorbed, due to the climb force is

$$W_n = \sigma_{z'z'}v_i = \sigma_{yy}v_i\sin^2\theta \qquad (A2)$$

where v_i is the atomic volume of a silicon interstitial.

The insertion of an interstitial to the fault requires additional work to compensate the other resolved stress $\sigma_{y'y'}$. This additional work is

$$W_i = \sigma_{y'y'}v_i = \sigma_{yy}v_i\cos^2\theta \qquad (A3)$$

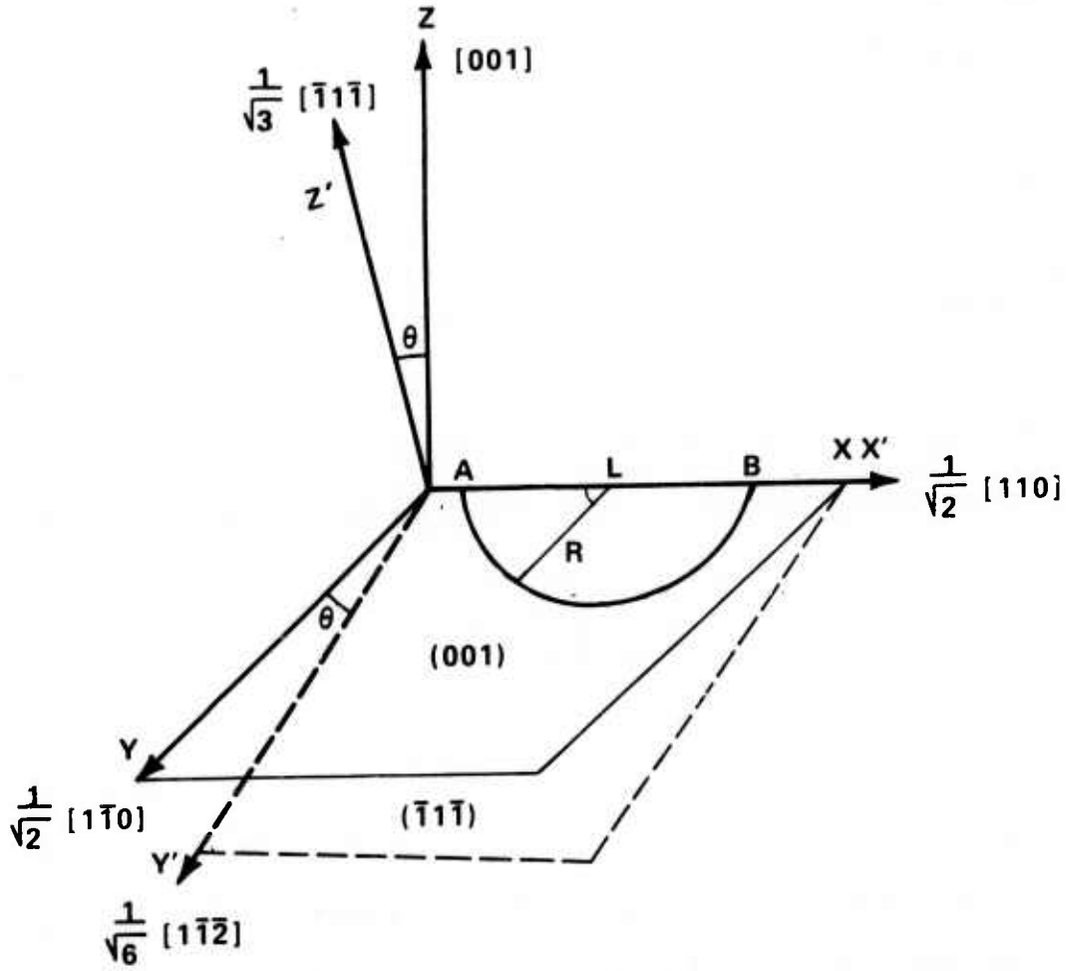


Fig. 7. A schematic diagram of a stacking fault lying in the ($\bar{1}1\bar{1}$) plane of a [001] oriented wafer.

The energy change associated with the line tension L, according to Ref. 22 is:

$$W_l = -\frac{Lv_i}{Rb} \tag{A4}$$

The energy change across a disk-shaped fault boundary according to Ref. 25 is:

$$W_f = -\gamma \frac{v_i}{R} \tag{A5}$$

where γ is the surface energy of a stacking fault.

The total energy change associated with the fault by absorption of an interstitial is obtained by adding Eqs. (A2) through (A5)

$$W = (\sigma_{yy} - \frac{L}{Rb} - \frac{\gamma}{R}) v_i \tag{A6}$$

The first term in Eq. (A6) causes the fault to grow and the second and third terms to contract. When R is smaller than a **critical size R_c, the terms describing fault contraction are dominant. Faults can be stabilized by large mechanical stresses or stresses due to precipitates. When R is larger than R_c, as in the present investigation, the growth term in Eq. (A6) is dominant.**

Thus the local equilibrium concentration of interstitials near the Frank dislocation is:

$$C_f = C_o \exp - \frac{\sigma v_i}{kT} \qquad (A7)$$

where C_o is the concentration of interstitials in local equilibrium with the oxidized surface, and σ_{yy} is expressed as σ for simplicity. The undersaturation of C_f relative to C_o is

$$C_f' = C_o - C_f \approx C_o \frac{\sigma v_i}{kT} \qquad (A8)$$

for $\sigma v_i << kT$. The undersaturation C_f' is assumed to be maintained with a distance $r = b$ of the partial dislocation. Far from the dislocation, C approaches C_o as r approaches ∞. The fault can be considered as a point sink in the region $r >> R$. This approach has been used in Ref. 22 to describe the climb of dislocation loops. The solution to the steady-state diffusion equation $\nabla^2 C = o$ is

$$C_o - C = C_f' \frac{b}{r} \qquad (A9)$$

The flux of interstitials diffusing to the fault and absorbed by it is

$$\frac{dN}{dt} = -2\pi r^2 D_i \frac{\partial C}{\partial r} = 2\pi D_i b C_f' \qquad (A10)$$

where D_i is the diffusivity of silicon interstitials.

The absorption of interstitials causes the fault to grow by an amount:

$$\frac{dR}{dt} = \frac{v_i}{Rb} \frac{dN}{dt} = \frac{2D_i v_i C' f}{R} \qquad (A11)$$

Using Eqs. (A1) and (A8), and the relations of $X = (Bt)^{0.5}$ and the self-diffusivity of silicon $D_s = C_o D_i v_i$, the growth rate follows as:

$$\frac{dR}{dt} = 2 \frac{D_s v_i K(B)^{0.5}}{R\ kT} t^{0.5} \qquad (A12)$$

The integration of Eq. (A12) from R = 0 at t = 0 yields

$$R = 2\left[\frac{v_i D_s K B^{0.5}}{1.5\ kT}\right]^{0.5} t^{0.75} \qquad (A13)$$

The fault length can be expressed as

$$l = 2R = A_o t^{0.75} \cdot \exp\left[-\frac{Q_{SD} + 0.5\ \Delta H_o}{2kT}\right] \qquad (A14)$$

and

$$A_o = 4\left[\frac{v_i D_o K B_o^{0.5}}{1.5\ kT}\right]^{0.5} \qquad (A15)$$

where A_o and Q_{SD} are the pre-exponential factor and the activation energy of self-diffusion D_s, respectively.

ACKNOWLEDGEMENT

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Chapter 2

LIFETIME CONTROL IN SILICON THROUGH IMPACT SOUND STRESSING (ISS)

by

G. H. Schwuttke and K. Yang

1. INTRODUCTION

Constant evolution of existing semiconductor device technologies aims simultaneously at large area device structures (chips) and at higher densities of substructures per chip. Such technological advances require corresponding penetration of new economic markets. This necessitates that device functions are developed that cost less per unit chip area. These economic considerations trigger new technological demands; for instance, the large area chips require the large diameter (76 mm) wafer. Further, the large area, high-density device structures and the companion large wafer generate new material requirements. Resistivity requirements in silicon are suddenly compounded because high-density substructures demand improvements in the micro-uniformity of resistivity. Smaller devices are less tolerant to micro-variations of resistivity. The same is true for variations of minority carrier lifetime.

Today, gross resistivity gradients for 76 mm diameter silicon wafers are specified in the 20% range. A sampling of commercially available silicon from major suppliers shows that micro-variations in resistivity are of the same order or even larger.

Similar variations in epitaxial silicon films are also present but smaller.

If it comes to lifetime control in today's silicon wafer, the situation can be totally unacceptable and order of magnitude variations are common on a slice, as well as from slice to slice. This is also true for epitaxial films.

While the device designer, in general, can cope with resistivity variations it becomes more and more difficult to manufacture large area high-density chips with acceptable cost due to large variations in generation lifetime encountered in silicon wafers and in epitaxial silicon films. Consequently, lifetime control in silicon wafers is one of the major research areas in today's silicon materials technology.[1]

This chapter discusses contract work related to this important field. In Part I of this report it was indicated that mechanical damage on a wafer surface can be used advantageously to influence or control minority carrier lifetime on the undamaged wafer surface. It was also pointed out that the technique of "Impact Sound Stressing" is useful in producing damage on a perfect silicon wafer surface. It was shown that ISS damage can be introduced in a controlled manner and thus lends itself to the application of lifetime control. Additional details of this work are reported in the following.

2. THE IMPACT SOUND STRESSING TECHNIQUE (ISS)

Impact Sound Stressing is useful in introducing mechanical damage into a semiconductor substrate under controlled conditions. To achieve "damage gettering" the damage is produced on the back face of the substrate before or between high temperature processing steps.

ISS can be applied repeatedly to the same substrate before or between different processing steps. Single or multiple ISS applications to the same substrate do not seem to enhance the probability of wafer breakage during handling or processing.

ISS provides controlled amounts of fresh lattice damage on the back face of an otherwise defect free silicon wafer. Thus it can be used to draw excess point defects to the wafer backside. Consequently, ISS of semiconductor substrates provides a potential not only for obtaining lower leakage currents in advanced silicon devices but also for obtaining higher semiconductor product yield and/or better product reliability.

3. PROCEDURE FOR ISS SURFACE DAMAGE GENERATION

The damage is induced in the silicon surface by impacting the wafer surface with 300 μm diameter tungsten balls under acoustic stressing. The acoustic stressing is done with a high intensity loudspeaker at the resonance frequency of the clamped

wafer, for instance at 1380Hz. Consequently, the tungsten balls impacting the wafer surface replicate an acoustic mode pattern of the clamped vibrating wafer through a damage pattern. The severity of damage thus achieved is determined by the vibration time, the number of tungsten balls on the wafer and by the power input to the speaker. The amount of damage introduced can be well controlled; thus wafer breakage is not a problem. The apparatus used for the sound stressing is shown schematically in Fig. 1. Accordingly, the wafer is coupled to an Atlas PD-60T 60 watt loudspeaker as used in public address systems. An approximately 30 cm long PVC pipe is used to couple the wafer to the loudspeaker.

The pipe is mounted to the speaker using the threads holding the loudspeaker trumpet which is dismounted for this purpose. The wafer is dropped into a recess made into the other side of the pipe and held in place with a teflon ring. A photomicrograph showing the mounted wafer loaded with 800 tungsten balls is seen in Fig. 2. To prevent loss of balls during vibration the surface of the teflon ring is covered with a piece of filter paper. Instead of the paper, a second wafer can be mounted in a tandem arrangement. The complete speaker assembly is mounted in a soundproof box. A MacIntosh M1-300 power amplifier is used to drive the unit. A Wavetek (Model 142) generator provides the square wave pulses.

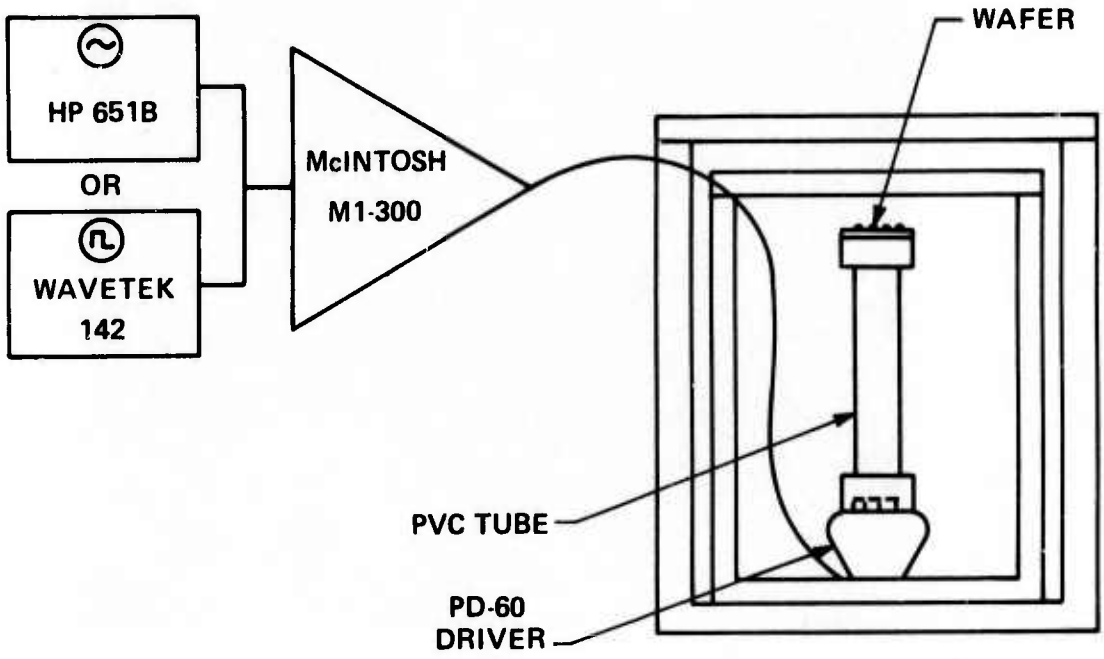


Fig. 1. Schematic of ISS setup.

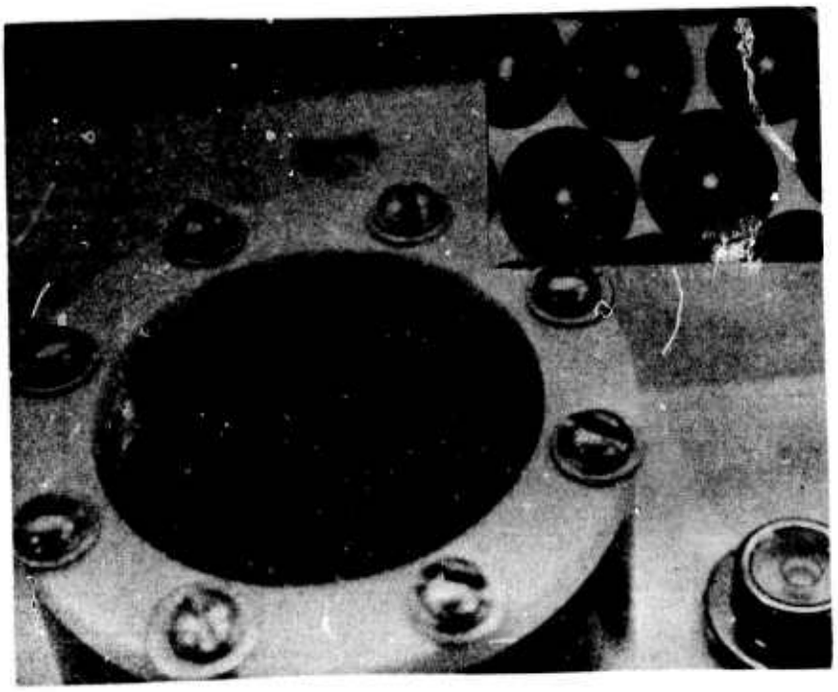


Fig. 2. Wafer loaded with 800 balls (single ball is 0.3 mm in diameter).

Examples of ISS'ed wafers are shown in the x-ray topographs of Fig. 3. The topograph shown in Fig. 3a is before stressing and reveals the high quality (zero dislocation) of the substrate used. Figures 3b through 3d are topographs of ISS'ed silicon wafers stressed at 12 watts, 40 watts, and 60 watts, respectively. The black contrast in the topographs reveals the damage distribution in the wafers. Note that the damage is not uniform across the wafer surface but localized in certain areas. With rising power the damage distribution covers more wafer area. A similar effect can be achieved by keeping the power constant but increasing the number of tungsten balls. The amount of damage produced is readily controlled by the number of tungsten balls vibrating on the wafer surface.

4. SURVEY OF ISS DAMAGE

ISS of silicon wafers produces two damage features: a fine, strongly directional abrasion leading to shallow grooves, and the formation of Hertzian fracture cones. Both features are displayed in the optical micrographs of Figs. 4a, b. The abrasion is more pronounced at low stressing power (Fig. 4a). The crack density increases dramatically with power input and is the leading feature at high power (Fig. 4b).

The grooves are bunched together in clusters and are indicated in the photomicrograph of Fig. 4a at positions marked A, B,

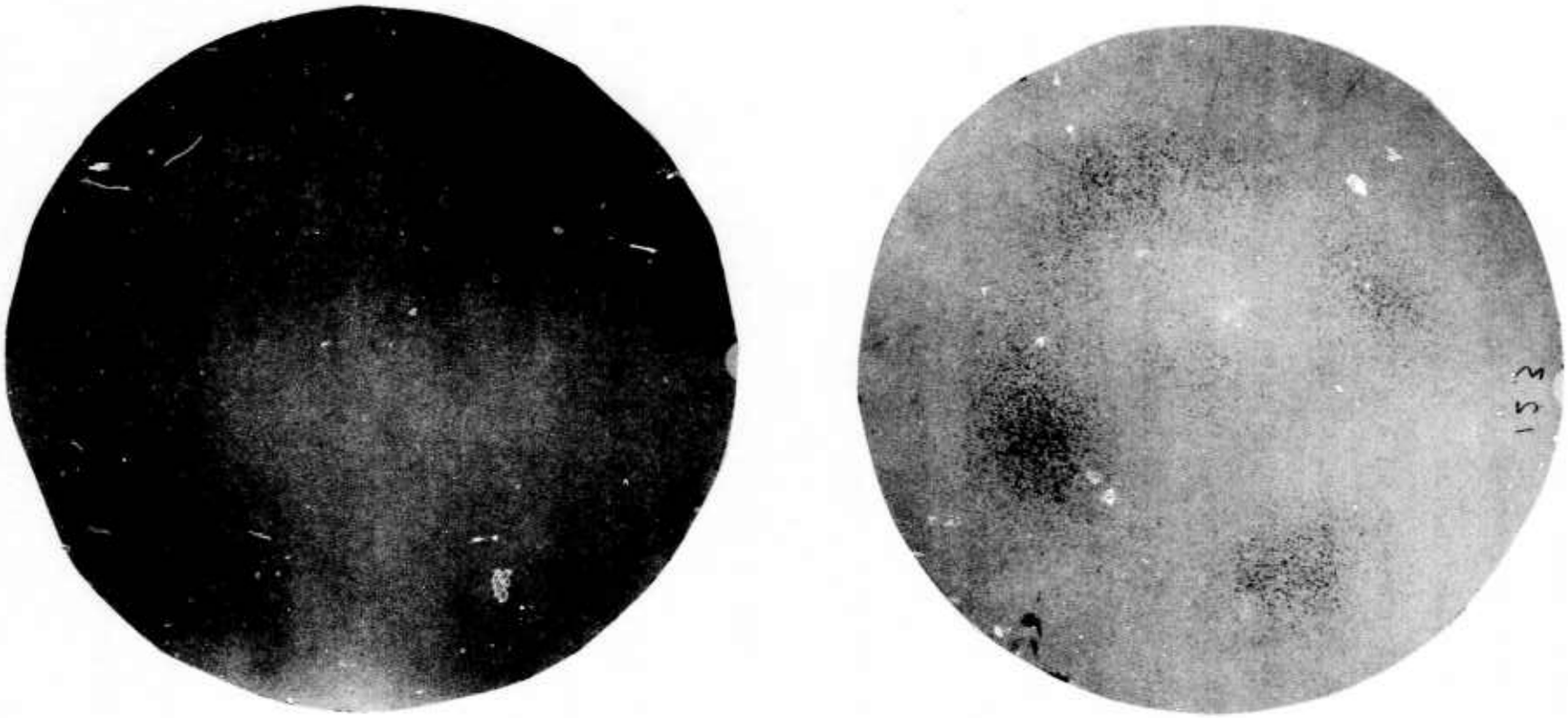


Fig. 3. X-ray topographs of silicon wafers
(a) Before ISS.
(b) ISS, 12 watts.

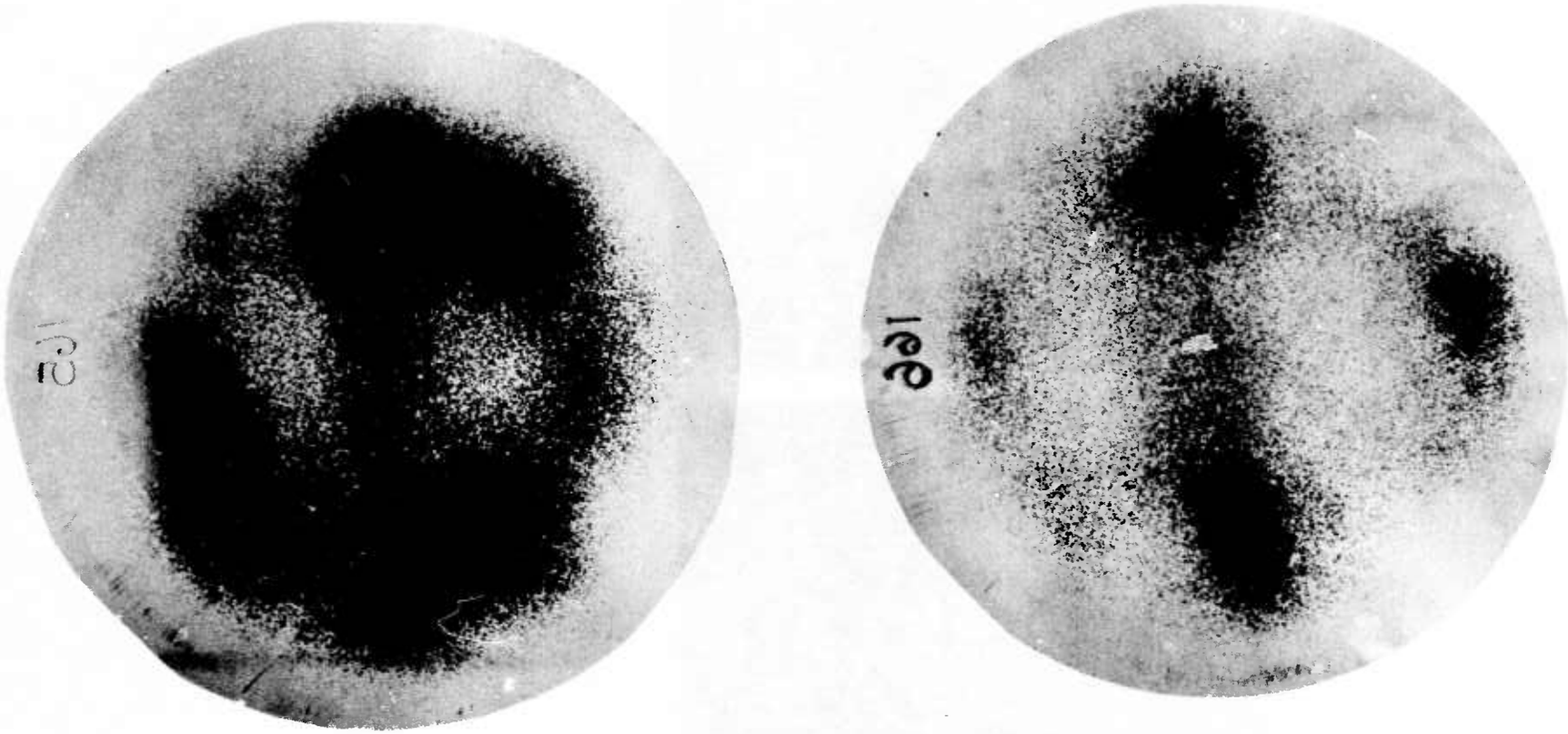


Fig. 3. X-ray topographs of silicon wafers
(c) ISS, 40 watts.
(d) ISS, 60 watts.

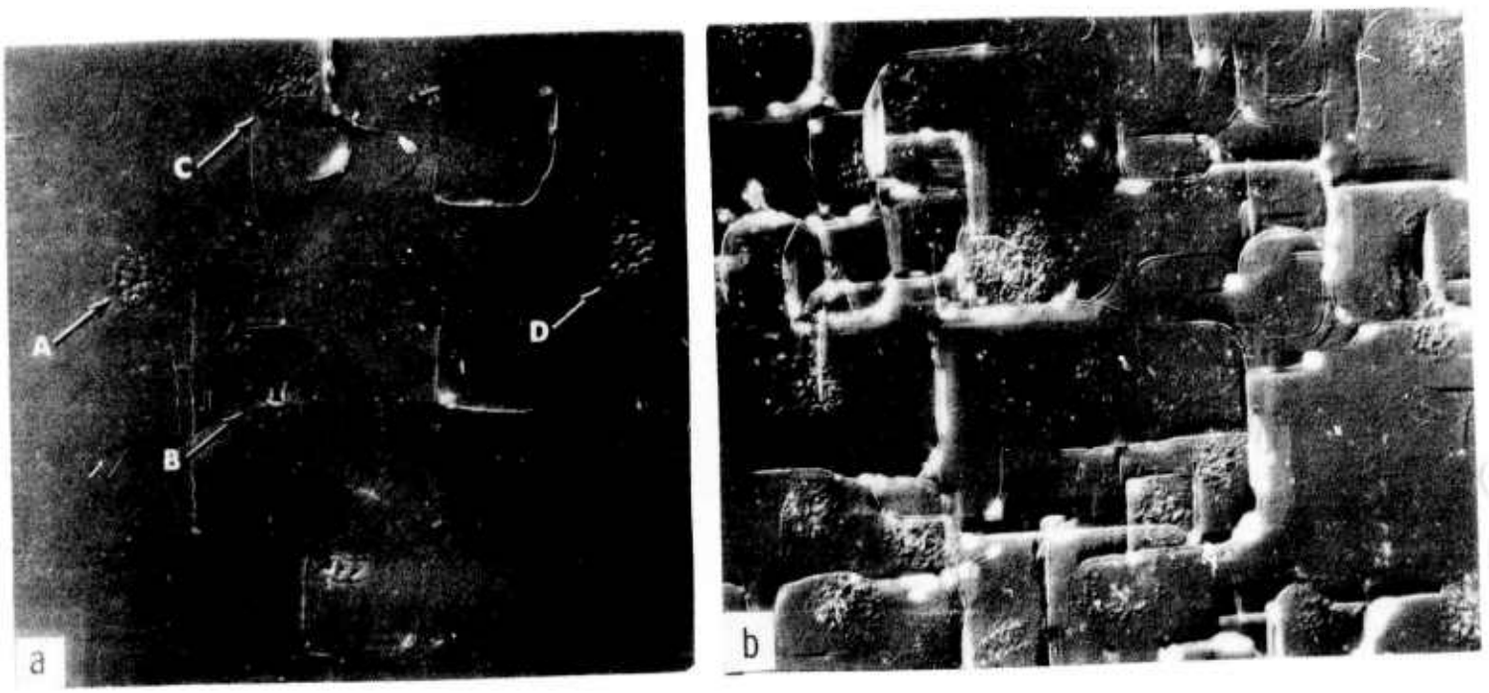


Fig. 4. Photomicrograph of ISS damage on wafer surface showing
(a) Abrasion (~370X).
(b) Fracture cones (~370X).

C, D. A scanning electron micrograph of such a damage cluster shows clearly their groove-like nature. An example is given in Fig. 5. A typical cluster area in the examples shown in Figs. 4 and 5 is approximately 10 to 15 μm^2 large and the density of grooves in a cluster is 1 per μm^2. A fracture cone measures approximately 50 μm along one side. The damage depth for the grooves is approximately 0.2 to 0.4 μm and for the fracture cones the depth varies from approximately 10 to 20 μm.

Detailed electron microscopy studies of both types of damage have been made and are discussed in Part I of this report.[2] A short summary of this work is given in the following:

Transmission electron microscopy of Hertzian fracture cones shows that cleavage at room temperature does not introduce dislocations into the silicon (Fig. 6). The crystal area surrounding the crack, including the crack tip, is free of dislocations (Fig. 7). Stresses around crack tips are not relaxed at room temperature. The terminating boundary lines of cracks in (001) silicon surfaces are located on (111) planes and run in <011> and <112> type directions. The cleavage plane for (001) silicon is (111) and (110) type. Moire patterns of cracks indicate that these cleavage planes are well developed. Cracks in (111) cleavage planes show Moire fringes which are strikingly similar to stacking fault fringes. This indicates that some cracks in silicon produce simple lattice displacements along (111) slip planes.

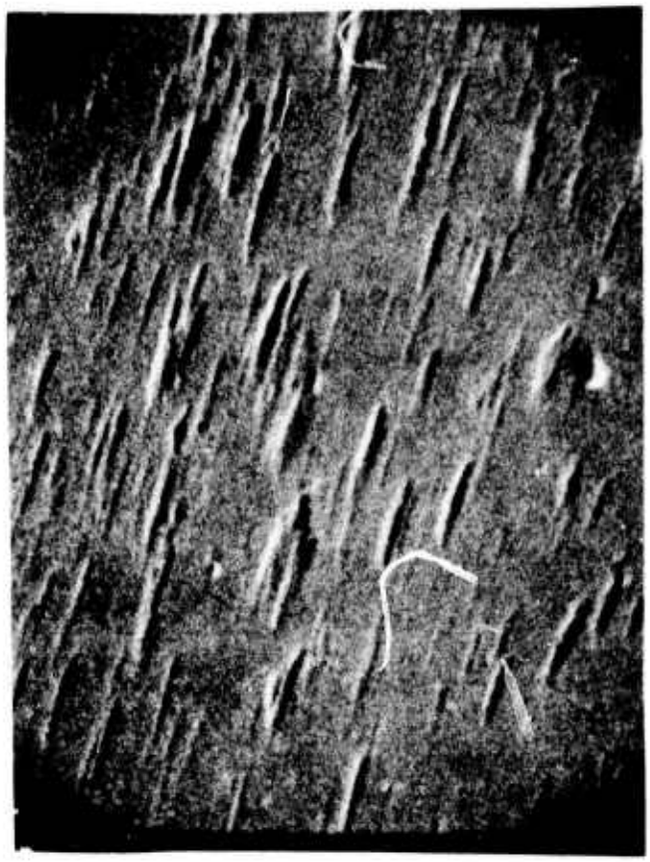
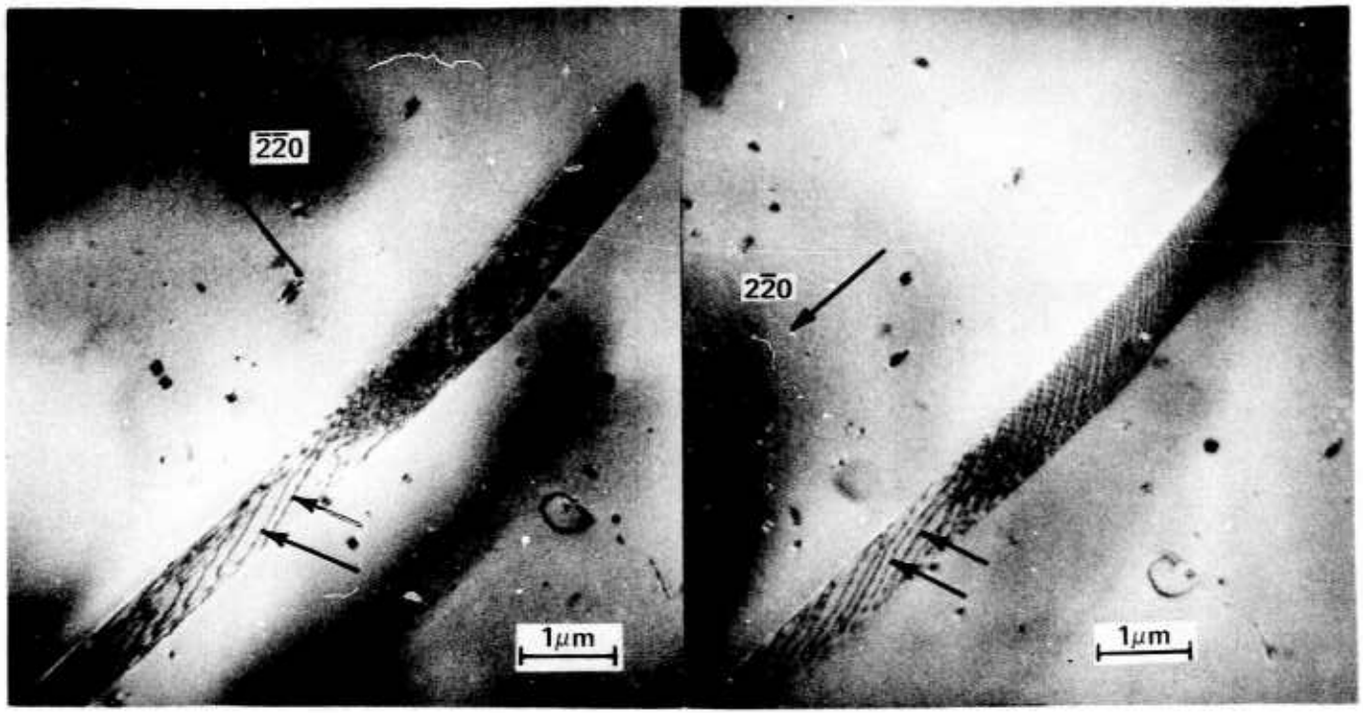


Fig. 5. SEM micrograph of damage cluster connected with abrasion.

Fig. 6. Transmission electron micrograph (TEM) of Hertzian fracture.



a b

Fig. 7. TEM of fracture cone tip after ISS. Note that crystal area outside of crack is free of dislocations. (a) g = $\bar{2}\bar{2}0$ and (b) $2\bar{2}0$ reflection.

Transmission electron microscopy of grooves shows that grooves are connected with dislocation bands (Fig. 8). The bands consist entirely of pile-ups of shear loops. The shear loops lie on (111) planes. The dislocation loops are composed of 60°-and 30°- dislocation segments with Burgers vector $[01\bar{1}]$ in the (111) loop plane. Dislocation bands of various densities are produced. Maximum densities observed are estimated to be as large as $10^{10}/cm^2$. Large dislocation pile-ups are connected with microsplits. Such splits are 1000Å in size or smaller (Fig. 9).

High temperature oxidation partially anneals the damage out of the crystal. Fracture cone annealing produces a dislocation network of 60°- and 90°- dislocations in the vicinity of the crack tips (Fig. 10). Low density dislocation bands anneal completely out of the crystal while high density bands produce stacking faults as an annealing product (Fig. 11). The stacking faults are extrinsic, bounded by a Frank partial with (a/3) (111) Burgers vector and are nucleated by submicron splits present in high-density dislocation pile-ups before annealing.

Damage propagation through the crystal towards the undamaged wafer surface before and after annealing does not occur. Therefore, ISS damage can be used advantageously to improve generation lifetime of minority carriers on the undamaged wafer surface. Such measurements are reported in the next section.

Fig. 8. TEM of abrasion clusters (grooves) post ISS. Note shear loop formation.

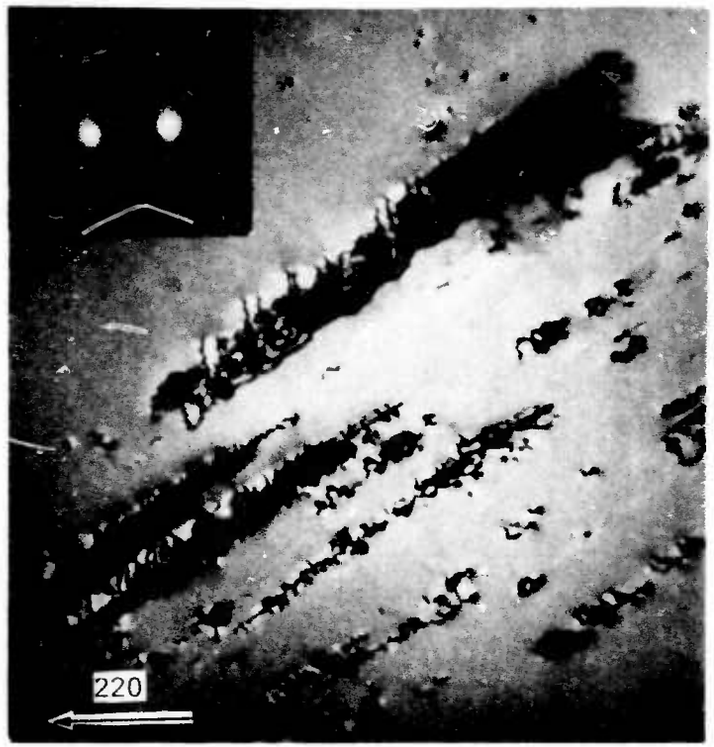


Fig. 9. TEM of high density shear loop pile-up connected with microsplits.

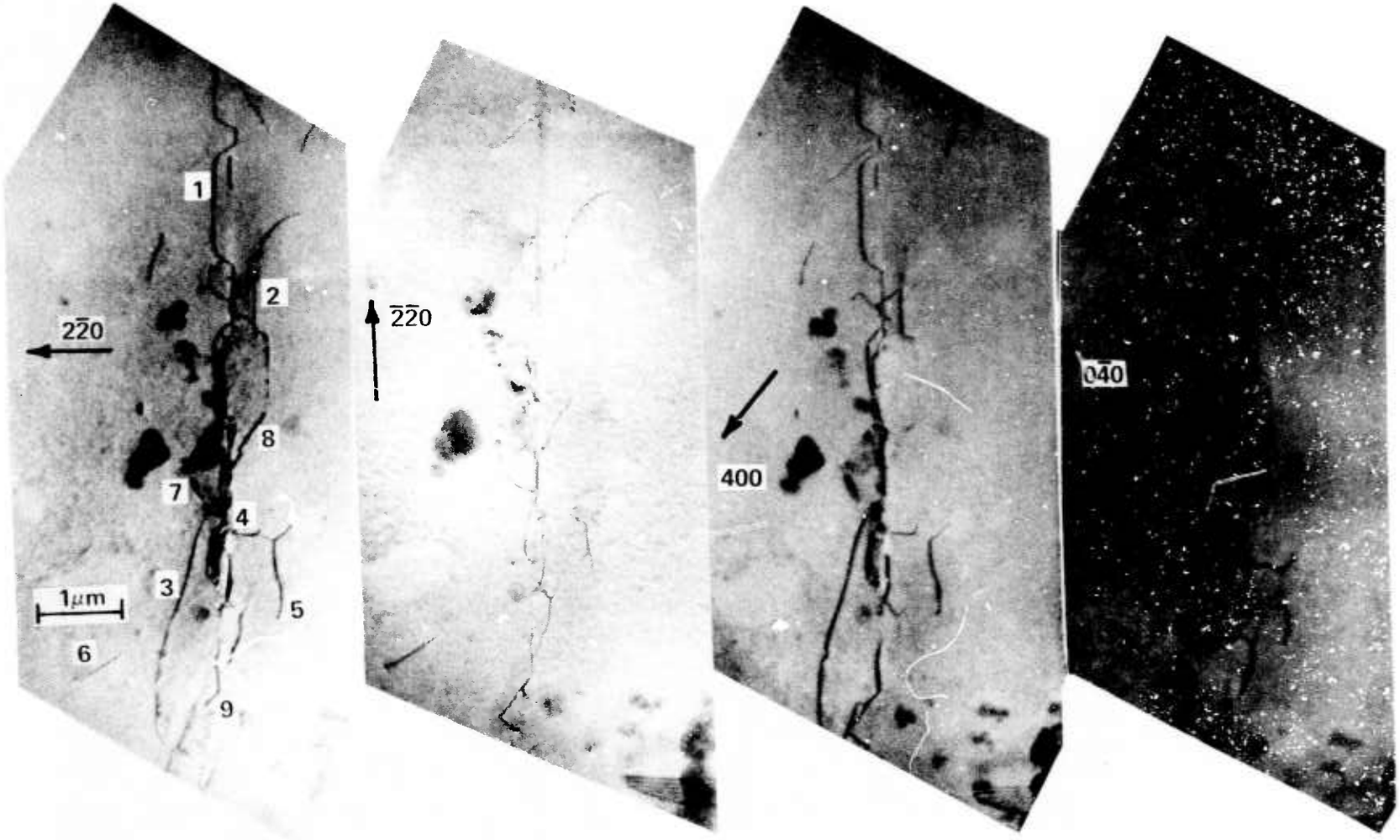
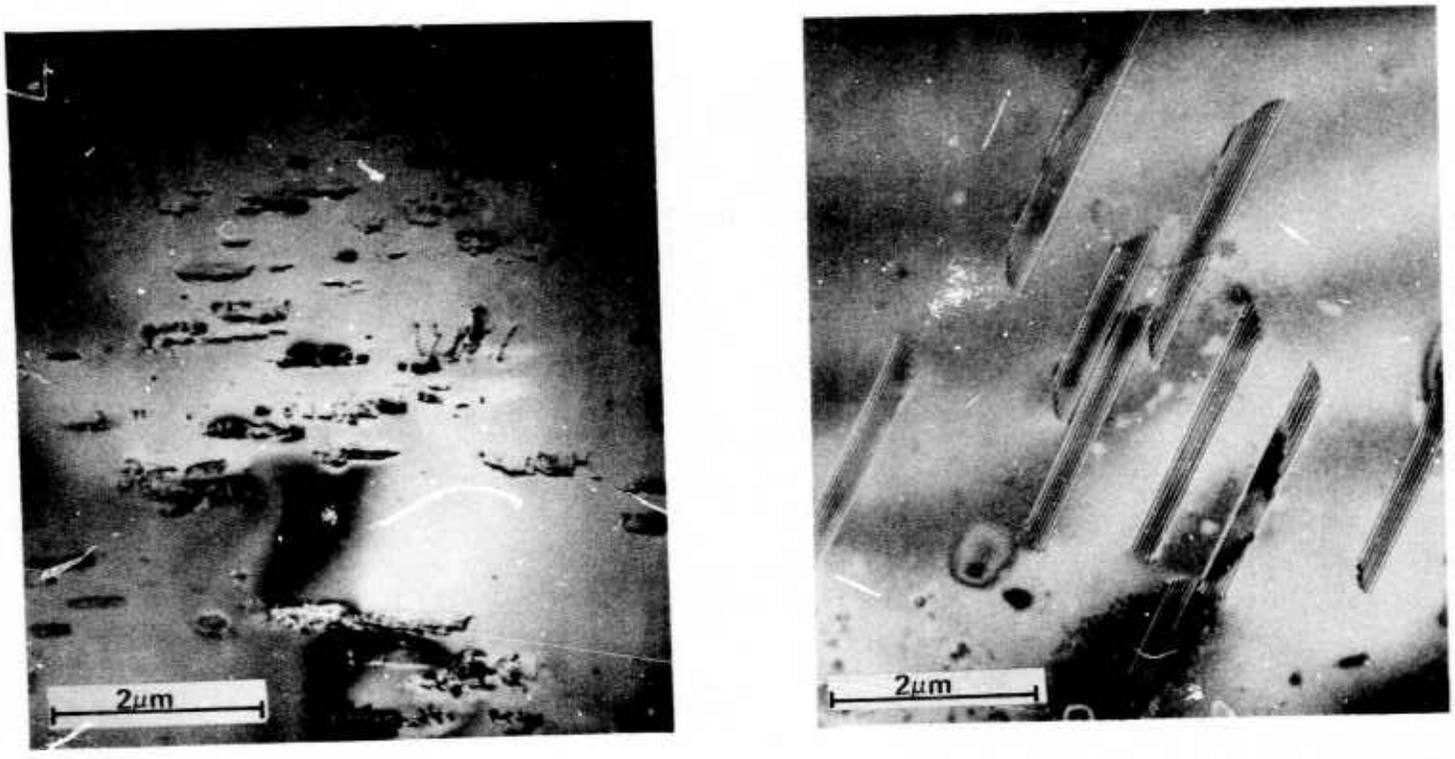


Fig. 10. TEM of fracture cone tip after oxidation. Note dislocation network.



a b

Fig. 11. TEM of abrasion area after oxidation. Note generation of stacking faults. (a) Before and (b) after oxidation.

5. LIFETIME IMPROVEMENT IN SILICON THROUGH IMPACT SOUND STRESSING

The finding that lattice damage at the wafer backside - opposite the device surface - can be utilized to achieve an increase of yield during semiconductor device processing is well documented.[3,4] Mechanisms for such damage-controlled yield improvements are also understood and relate to the Cottrell interaction that occurs between the different modes of lattice damage.[5] Elastic interaction between dislocations and point defects in the silicon lattice is such that point defects are always drawn to the dislocations. Consequently, fresh lattice damage introduced in a controlled manner on a wafer backside can be used as a "broom" to sweep the device side of the wafer clean of excess point defects and thus diminish undesirable clustering effects and other crystal defect formation during device processing. A direct result of this gettering effect is a marked improvement of minority carrier lifetime measured close to the wafer surface and a strong reduction in the number of crystallographic defects normally produced during high temperature device processing.

Impact Sound Stressing is a simple but elegant tool that makes "damage gettering" controllable and thus applicable to device manufacturing. The following results are in support of this statement.

5.1 Experimental

Substrates used in the context of this work are of (001) orientation and 76 mm diameter. They are p-type, 2 to 20 ohm resistivity and sliced from Czochralski grown crystals. Two different quality classes of wafers are used. The first class contains wafers selected for their excellent lifetime distributions. The lifetime in such wafers is long and covers approximately a range from 1 μsec to ≈ 500 μsec. Histograms[6] showing the typical lifetime distribution of such selected wafers are shown in Fig. 12. The second quality class is called standard and covers lifetime distributions in the range from 0.01 μsec to 1 μsec. Lifetime histograms typical for standard wafers are given in Fig. 13. The terms "selected" or "standard" have no commercial meaning. They are used only for easier and clearer presentation of our data.

The silicon wafers are ISS'ed on their backsides as discussed in Section 2 of this chapter. The lifetime measurements are made using the MOS - capacitor technique described by Fahrner and Schneider.[7]

After ISS and after any additional processing, such as epitaxial deposition or ion implantation, the silicon slices are processed to contain 36 circular MOS capacitors. Each device is 1.5 mm in diameter. A 5000Å thick oxide is grown

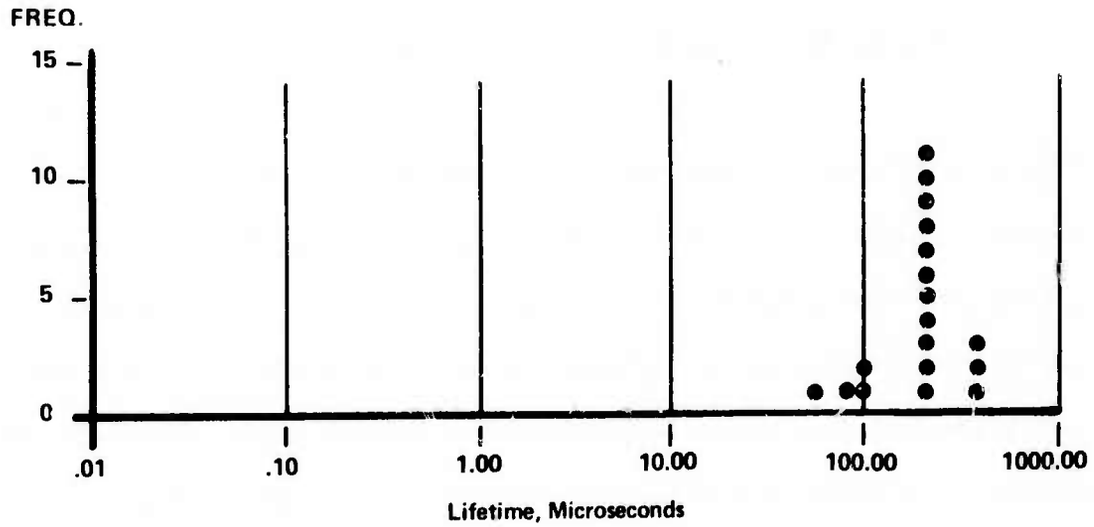


Fig. 12. Lifetime distribution histogram of selected wafers.

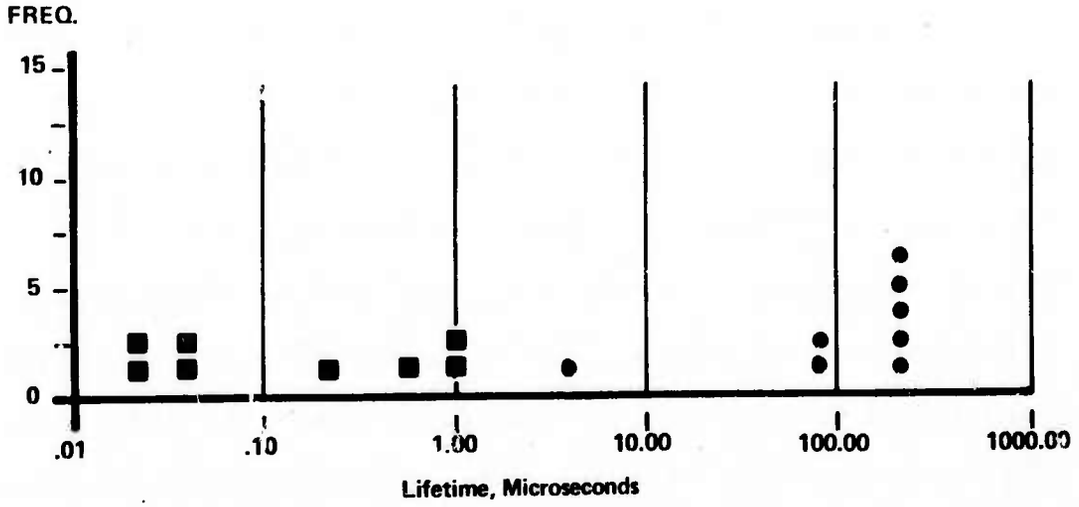


Fig. 13. Lifetime distribution histogram of standard wafers.

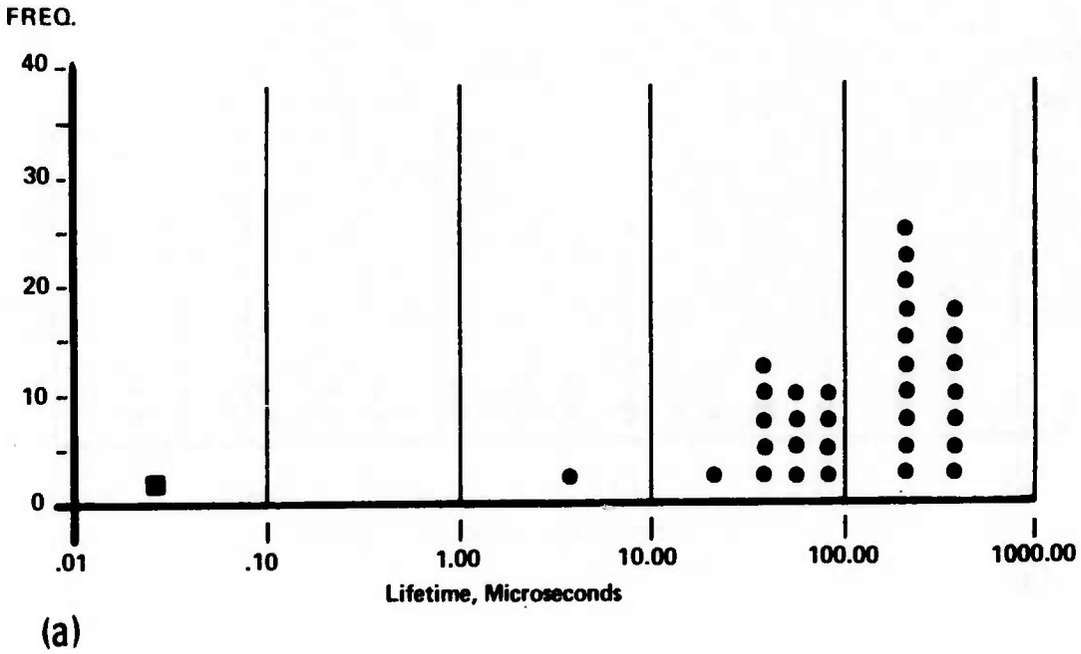
at 1000°C using a dry-wet-dry oxidation cycle. Aluminum metallization is used. After metallization the wafers are annealed for 15 minutes at 400°C. Surface state density after annealing is below 10^{10} $[eV^{-1}cm^{-2}]$.

Three different experiments are reported. The first one demonstrates lifetime improvements achieved in silicon substrates, the second one discusses lifetime improvements obtained in epitaxial silicon grown on ISS'ed silicon substrates, and the third experiment presents lifetime improvements achieved in epitaxial silicon films grown directly on ion-implanted silicon surfaces.

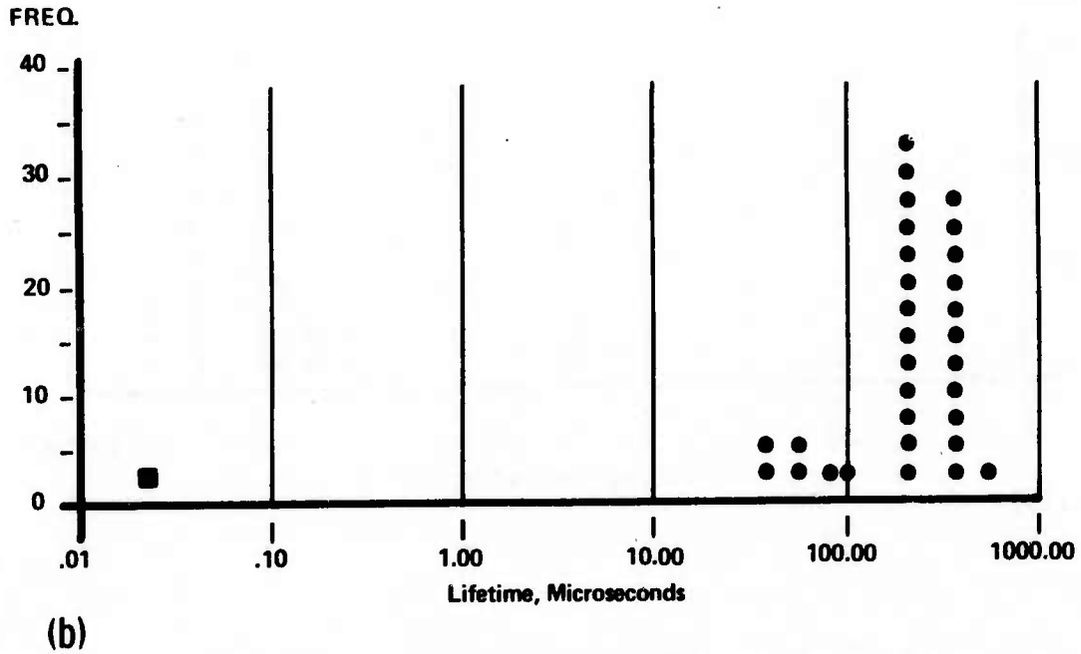
5.2 Results

5.2.1 Substrates

Results summarizing the influence of ISS damage on substrates are given in the histograms of Figs. 14 and 15. Figure 14 gives data obtained on "selected" wafers and Fig. 15 gives the data obtained on "standard" wafers. According to Fig. 14, ISS stressing of high-quality wafers does not degrade the minority carrier lifetime in such wafers. It is apparent that such wafers display a tendency to smaller variations in their lifetime range. The improvement in lifetime obtained through ISS of standard wafers appears clearly in the histograms of Fig. 15. Wafers with their maximum lifetime distribution below 1 μsec show a definite shift to the longer lifetimes above 1 μsec.



(a)



(b)

Fig. 14. Lifetime distribution histogram of selected wafers

(a) Not ISS'ed.
(b) ISS'ed.

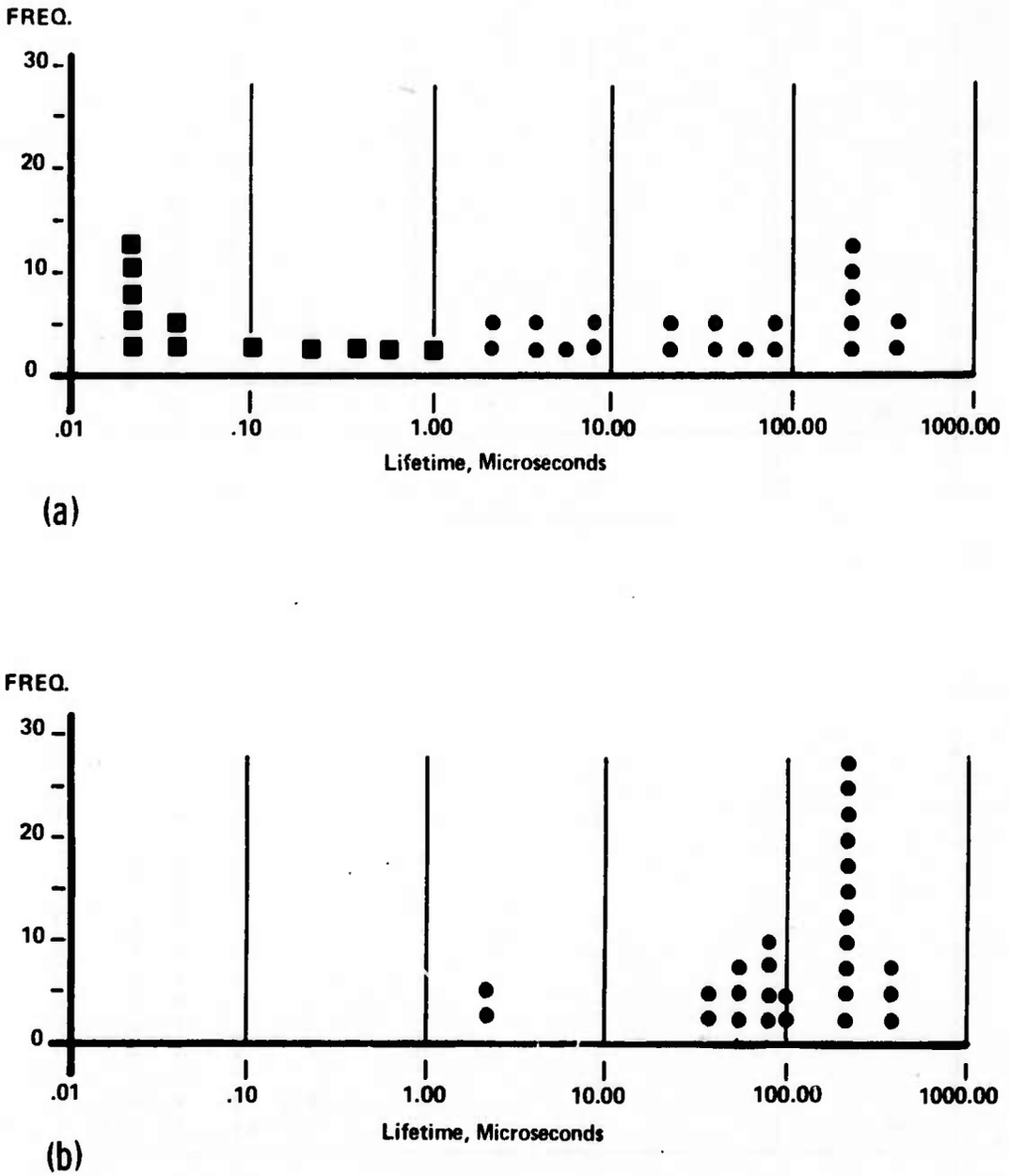


Fig. 15. Lifetime distribution histogram of standard wafers

(a) Not ISS'ed.
(b) ISS'ed.

Experiments were also performed to test if such lifetime improvements are lost during subsequent oxidation cycles. Three oxidation cycles were performed. Each time the capacitors (oxide, Al) were removed for reprocessing of the wafer. No degradation in lifetime improvement occurred. In another experiment the capacitors were removed and the wafer back was again ISS'ed before the subsequent oxidation step. This was also done three times. No lifetime degradation occurred in such wafers.

5.2.2 Epitaxial Films on ISS'ed Substrate

The n-type epitaxial films are grown on 15 ohm-cm, (001), p-type substrates by the hydrogen reduction of $SiCl_4$ at 1100°C. The films are 6 μm thick. The dopant (arsenic) concentration in the film ranges from 0.8 to 1.6 10^{16} As atoms/cm^3. The substrates are ISS'ed on the backside prior to epitaxy. After the epitaxial deposition a dry oxide, 1400Å thick, is grown on the epitaxial film at 1100°C. The minority carrier lifetime in the film is measured according to Ref. 7 using capacitors of 0.5 mm in diameter. Lifetime distributions obtained in such epitaxial films are given in Figs. 16 and 17.

The measurements indicate that ISS is also effective in improving minority carrier lifetime in epitaxial silicon.

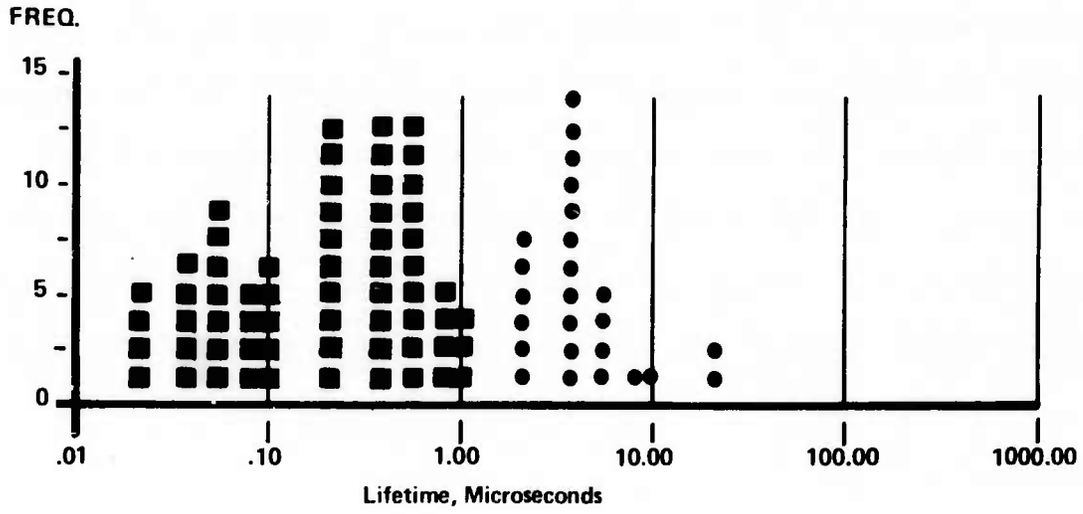


Fig. 16. Lifetime distribution histogram of epitaxial wafers, substrate not ISS'ed.

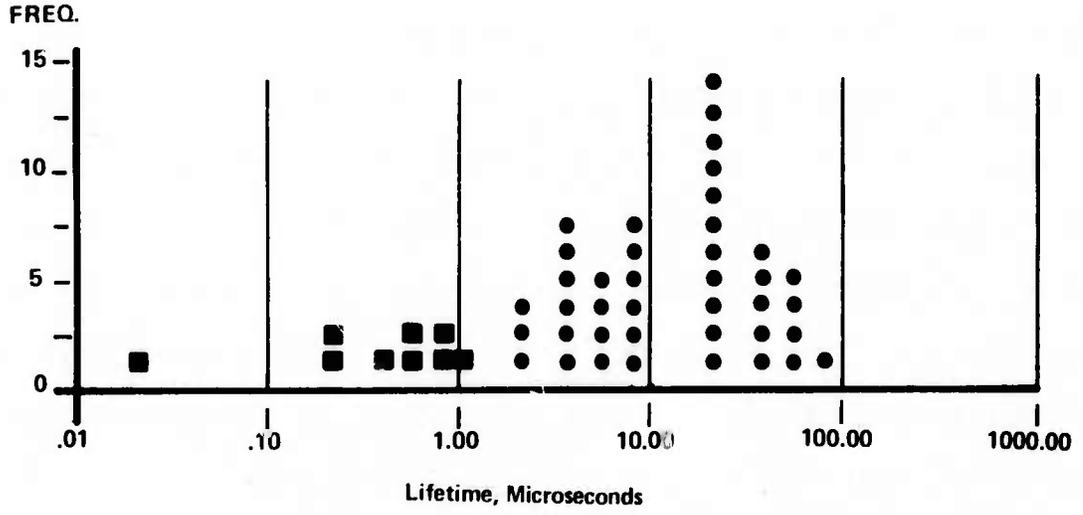
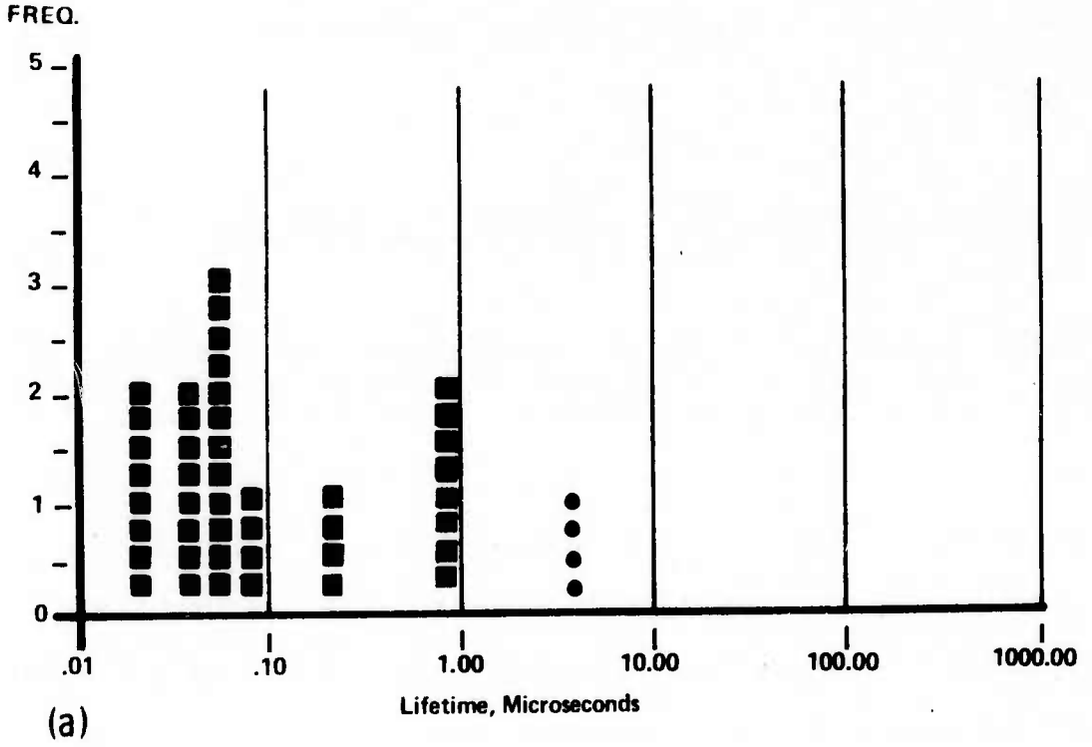


Fig. 17. Lifetime distribution histogram of epitaxial wafers, substrate ISS'ed.

On the average an epitaxial silicon lifetime of ∿ 15 μsec is obtained.

5.2.3 Epitaxial Films on Ion Implanted Substrates

Epitaxial silicon grown on an ion-implanted surface normally shows a high stacking fault density and a low lifetime. ISS of substrates can reduce the defect density in such epitaxial films and thus improve the lifetime. This is shown in the following. Two different sets of wafers are used for this experiment. The first set contains backface ISS'ed substrates while the wafers in the second set are free of ISS damage. Both sets of wafers are ion implanted on the front side with 80 keV As^+. The implantation is done over half the wafer area only. Thus, each wafer is divided into an implanted and into a non-implanted area. After ion implantation the wafers are processed in the epitaxial reactor. After epitaxial deposition (6 μm) MOS capacitors are formed on the epitaxial film and lifetime measurements are made. The data obtained are for an implantation dose ranging from 10^{13} As^+/cm^2 to 10^{16} As^+/cm^2. Typical lifetime data obtained are given in Figs. 18, 19. Figure 18 summarizes lifetime data obtained on a wafer not Impact Sound Stressed, while Fig. 19 summarizes the data obtained on the ISS'ed wafer. Figures 18a and 19a represent the wafer halves not implanted while Figs. 18b and 19b show lifetime data on the implanted ($10^{13}/cm^2$) wafer halves. Two things are



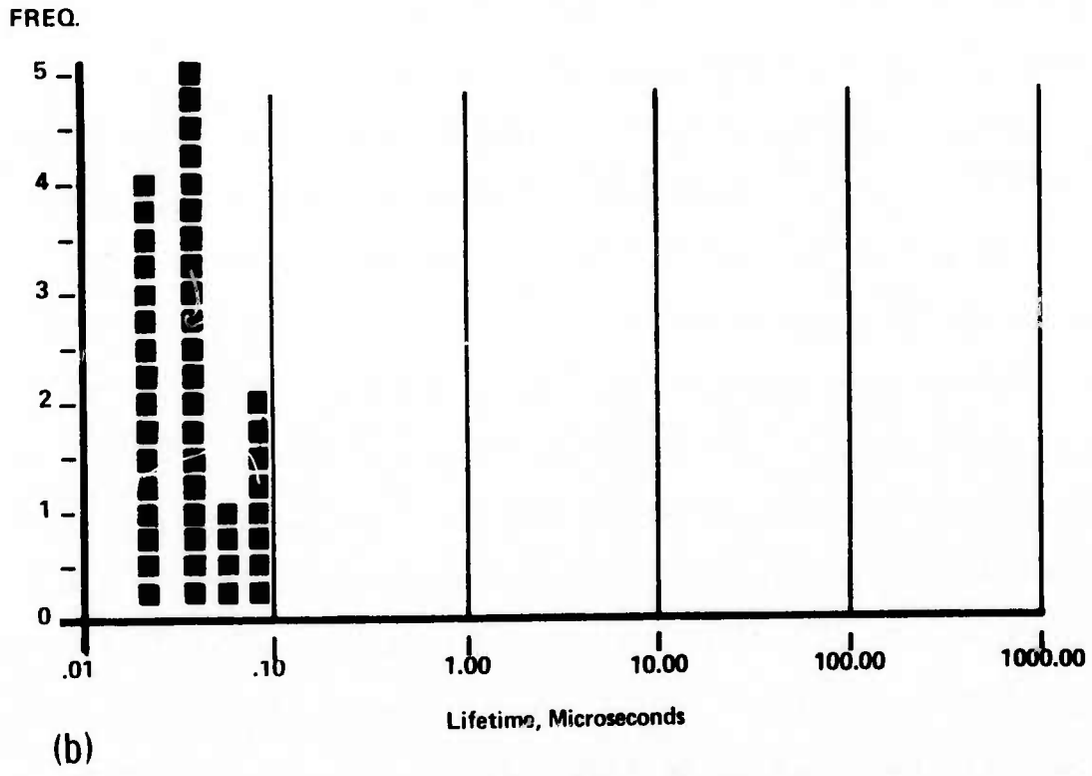


Fig. 18. Lifetime distribution histogram of epitaxial wafer, grown on ion-implanted surface, substrate not ISS'ed. (a) No implantation. (b) As^{+} $10^{13}/cm^{2}$ implantation.

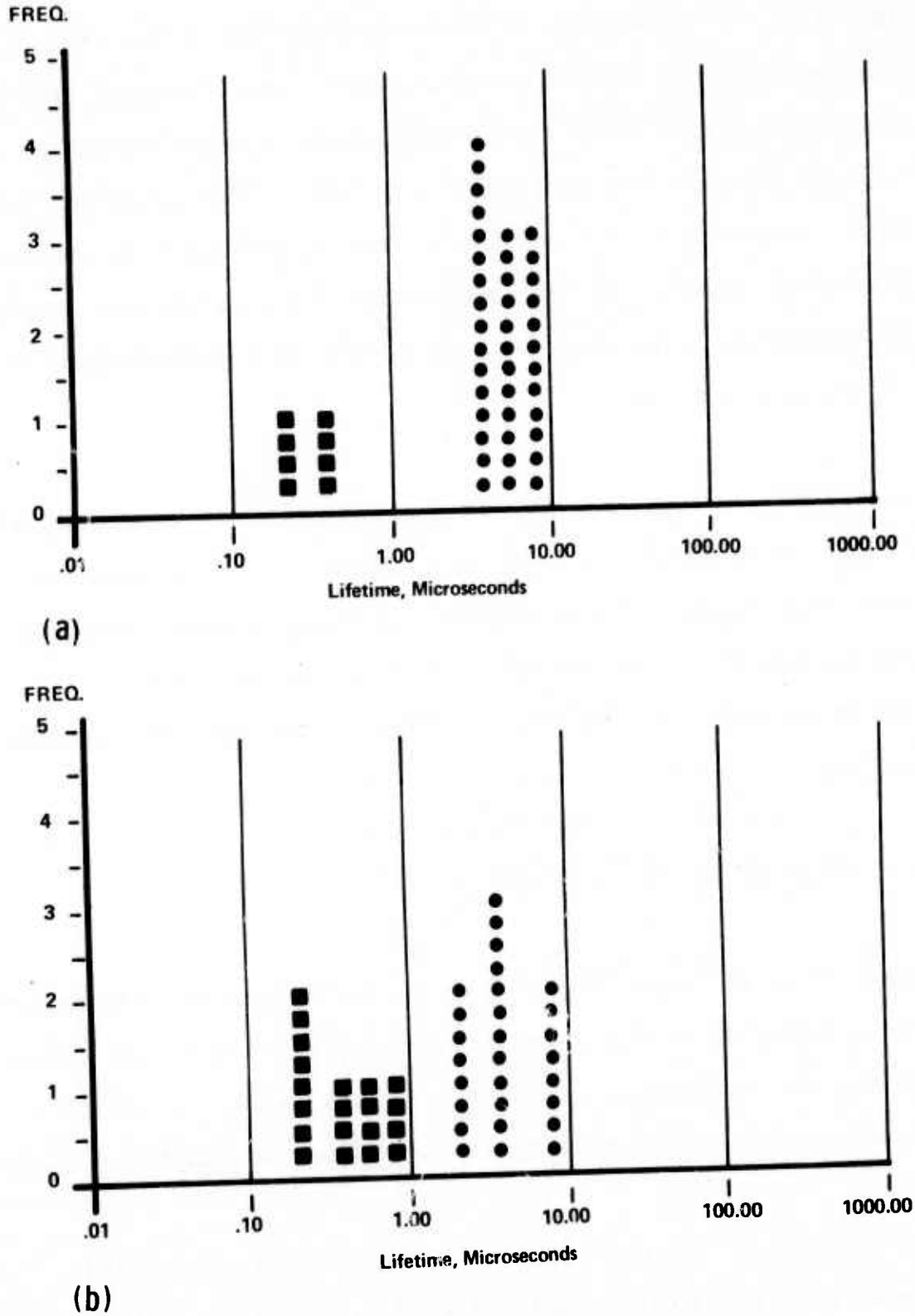


Fig. 19. Lifetime distribution histogram of epitaxial wafer, grown on ion-implanted surface, substrate ISS'ed (a) No implantation. (b) As^{+} $10^{13}/cm^{2}$ implantation.

apparent. A comparison of Figs. 18a and 18b shows that ion implantation before epitaxial deposition reduces the lifetime in the epitaxial film. This reduction in lifetime can be reduced through the application of ISS before epitaxial film deposition (Figs. 18b and 19b). The measurement on the not implanted halves confirms again that ISS can improve lifetime in epitaxial films when applied before film deposition (Figs. 18a and 19a).

Interesting is the low defect density obtained in epitaxial films. This effect is very pronounced for films grown on high dose implanted substrates. An example which compares the perfection of an epitaxial film grown on a substrate implanted with 10^{15} As^{+}/cm is shown in the photomicrographs of Fig. 20.

6. DISCUSSION

Generation lifetime is strongly influenced by crystal defects. The success of backside Impact Sound Stressing in improving generation lifetime in silicon surfaces is the result of a reduction of defect density in the device active wafer surface.

To assess the defect state in the wafer surface the MOS capacitors are removed and the surface is Sirtl etched. The defects present in the surface are optically visible due to preferential etching. Thus, it is possible to count the

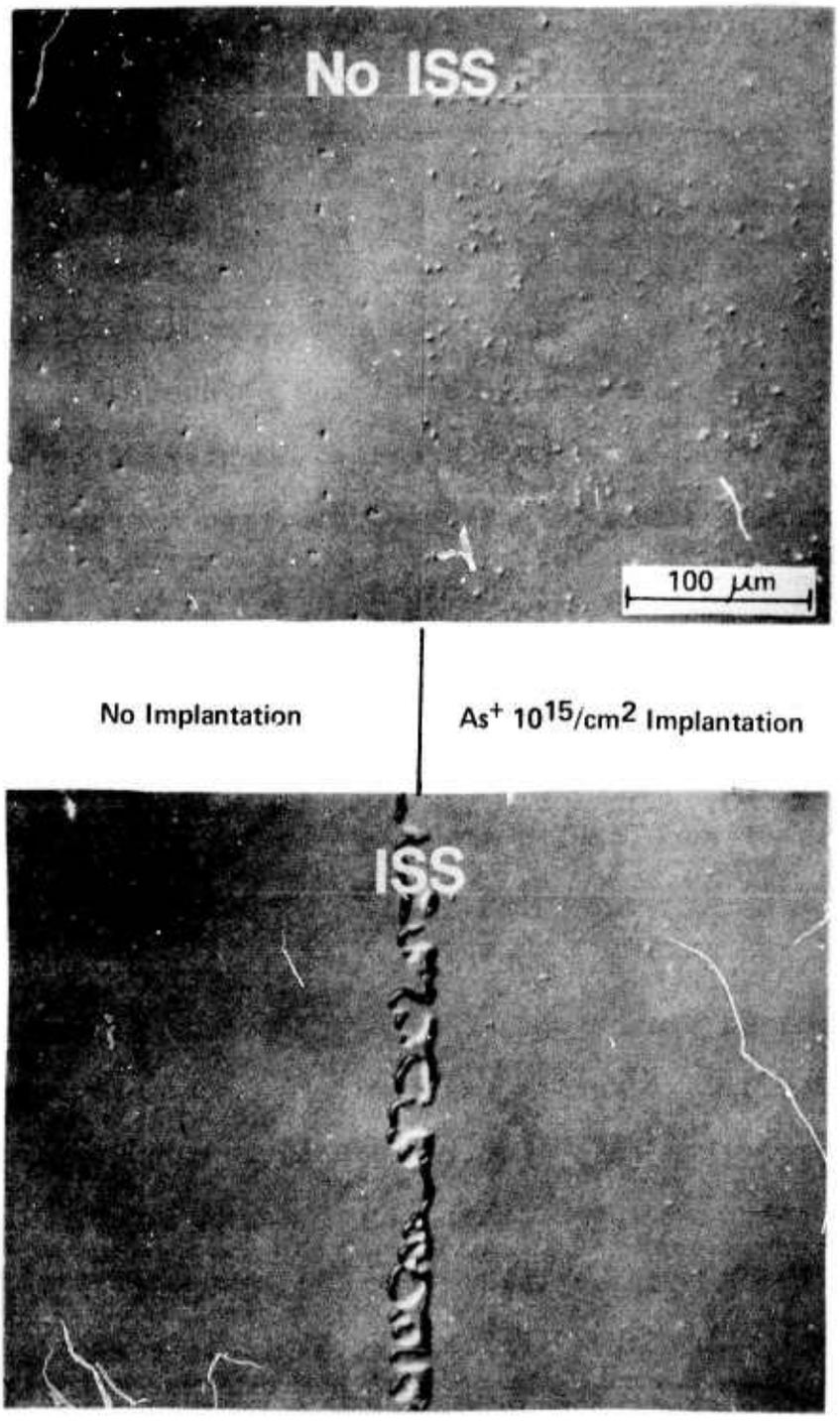
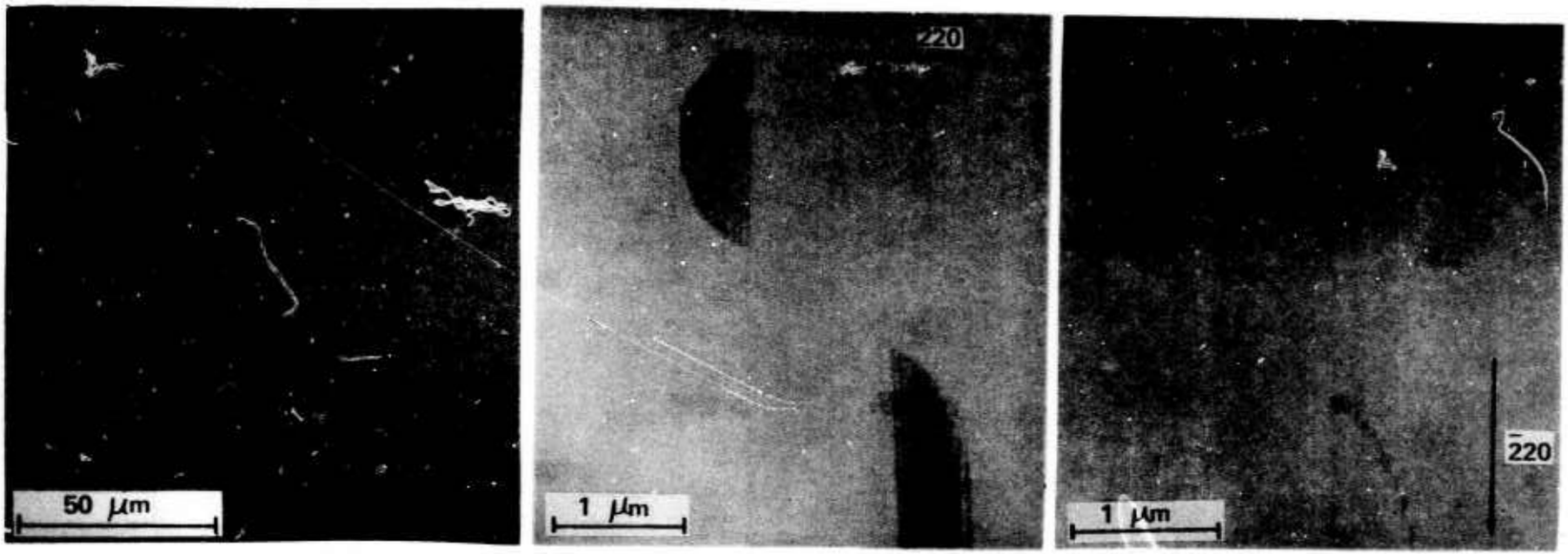


Fig. 20. Photomicrographs of defect density in epitaxial layer, grown on ion-implanted substrate. Note reduction of defect density through ISS in implanted area.

defects in areas previously occupied by MOS capacitors; therefore, a direct correlation between defect density and measured lifetime is possible.

The main defects in substrates are oxidation-induced stacking faults. They are easily identified by their Sirtl etch pattern. A typical example of such a fault, identified by its optical micrograph and its transmission electron microscopy image, is given in Figs. 21a, b, c.

Main defects in the epitaxial silicon are (a) grown-in stacking faults, (b) oxidation-induced stacking faults, and (c) mounds. Examples of such faults are shown in the photomicrographs of Figs. 22 and 23. After etching, the grown-in faults display the well-known "square" figure which results from the intersection of the four faulted planes with the (001) surface. Their density in the epitaxial film is quite low ($10/cm^2$). The oxidation-induced stacking faults in the epitaxial films are very similar to the faults observed in oxidized substrate surfaces. They are also of the Frank type (extrinsic). The mounds observed in the epitaxial films are partially developed stacking faults. They are smaller than standard oxidation-induced stacking faults. The reason for their small size has not been investigated in the context of this work and is presently not understood. However, it was noted that an HF treatment of the epitaxial surface before oxidation caused the mounds to develop into standard oxidation type stacking faults.



a b c

Fig. 21. Epitaxial oxidation stacking fault.

(a) Optical micrograph.
(b) TEM $\underline{g} = \underline{2}20$.
(c) TEM $\underline{g} = \bar{2}20$.

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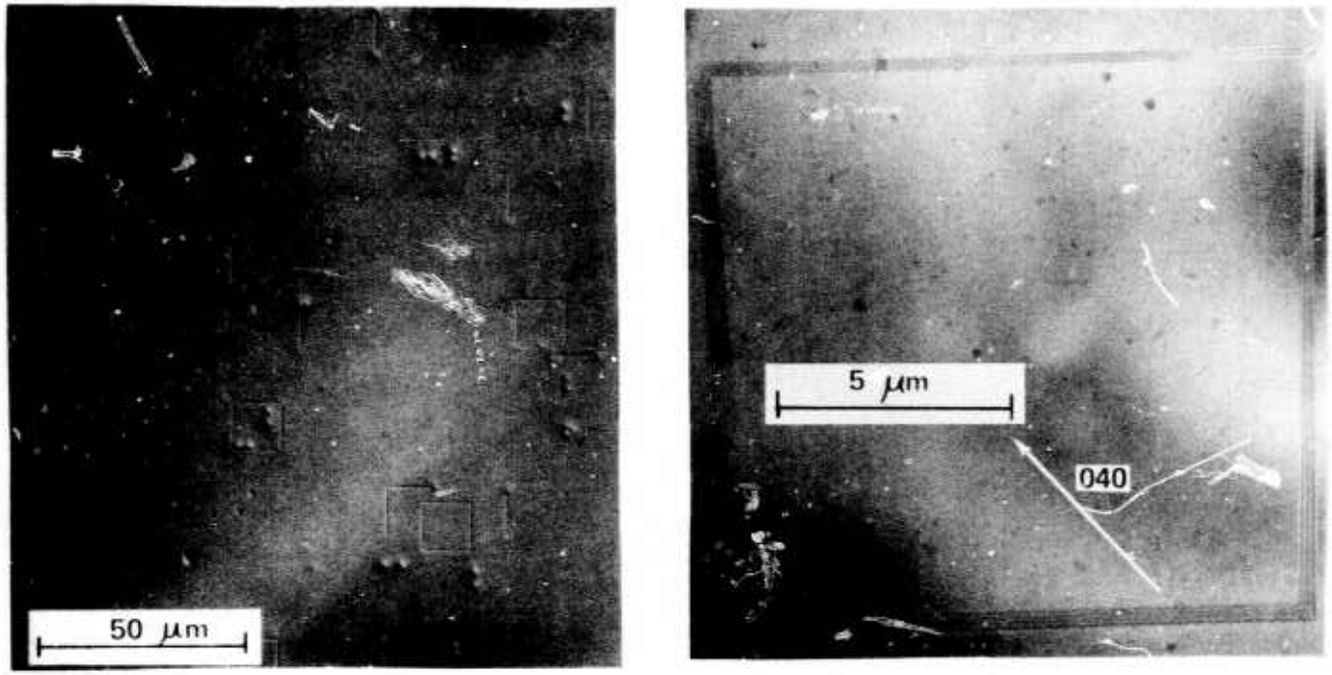
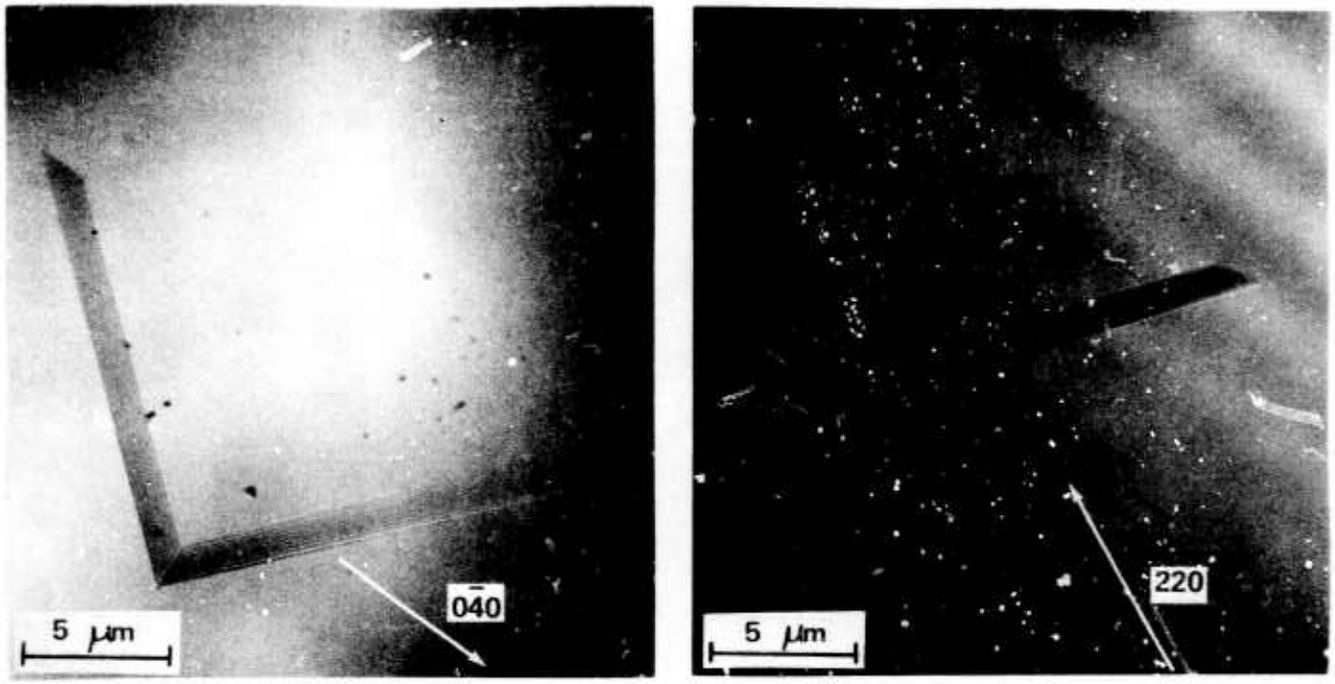


a b

Fig. 22. Epitaxial stacking faults.

(a) Optical micrograph.
(b) TEM of single square-type fault.



c d

Fig. 22. Epitaxial stacking faults.

(c) TEM of L-shaped type.
(d) TEM of linear type.

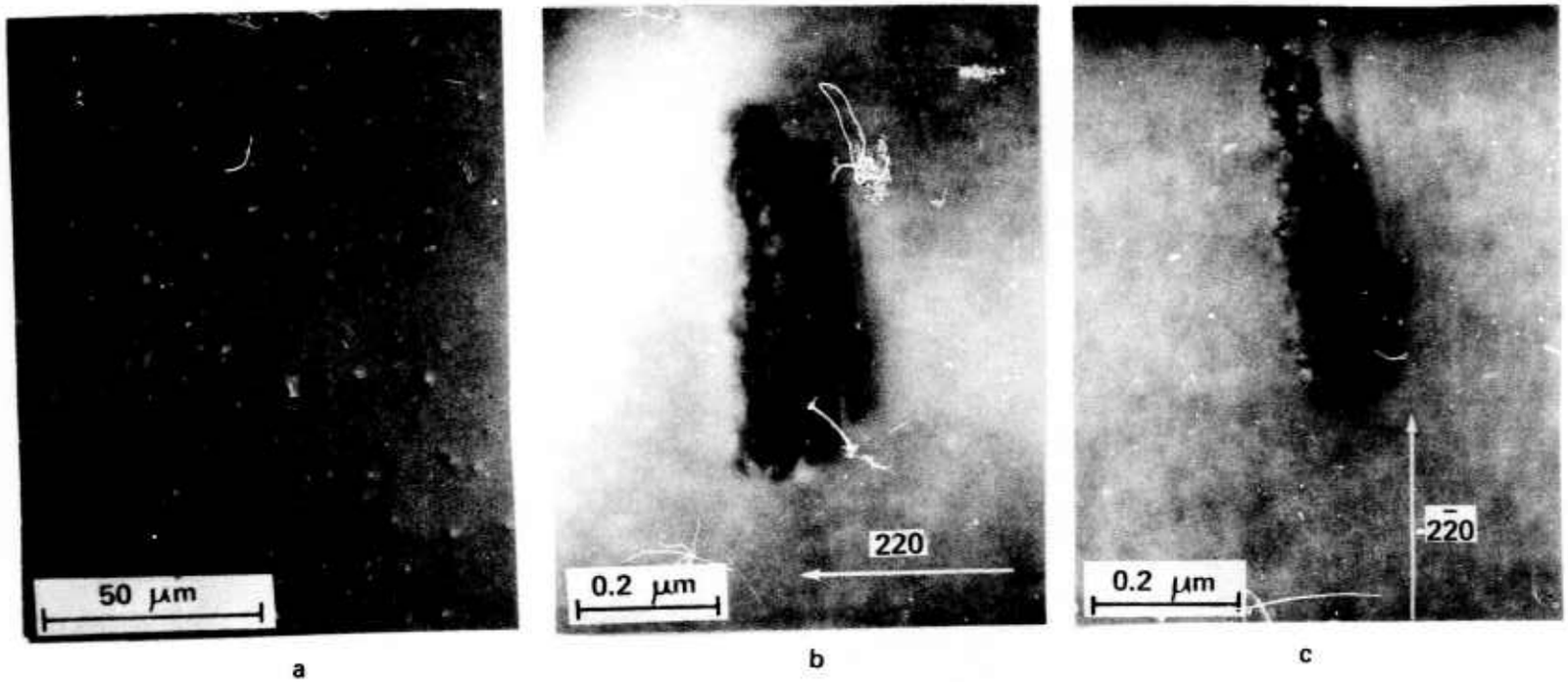


Fig. 23. Epitaxial mound defect.

(a) Optical micrograph.
(b) TEM g = $2\bar{2}0$.
(c) TEM g = $\bar{2}20$.

The defect density found in epitaxial silicon covers quite a large range. This range made it possible to obtain a fairly accurate lifetime vs. defect correlation. The lifetime data corresponding to the epitaxial samples of Figs. 16 and 17 were correlated with the defect density found under every single MOS dot. The lifetime vs. defect dependency thus obtained for the samples is given in Fig. 24. In making this correlation it was observed that practically all MOS dots, free of defects after Sirtl etching, had a lifetime between 10 to 100 μsec. A rapid decrease in lifetime was noted with the number of defects present under each MOS dot. Another general finding is that oxidation-induced stacking faults are more detrimental to lifetime than mounds. It was also noted that backside ISS'ed wafers exhibited a considerably lower defect density and a longer lifetime than non-stressed wafers.

Using the method of linear regression, a best fit of the data summarized in Fig. 24 is obtained. The curves are plotted in Fig. 24. Accordingly, one obtains the following correlation between lifetime and defect density. For oxidation-induced stacking faults:

(1) $t = A_1 d_{st}^{-1.05}$

For oxidation-induced mounds:

(2) $t = A_2 d_m^{-1.04}$

t = generation lifetime in microseconds; A_1 and A_2 constants

d_{st} = number/cm^2 of oxidation-induced stacking faults

d_m = number/cm^2 of oxidation-induced mounds

The correlation coefficient is -0.775 for oxidation stacking faults and -0.707 for mounds.

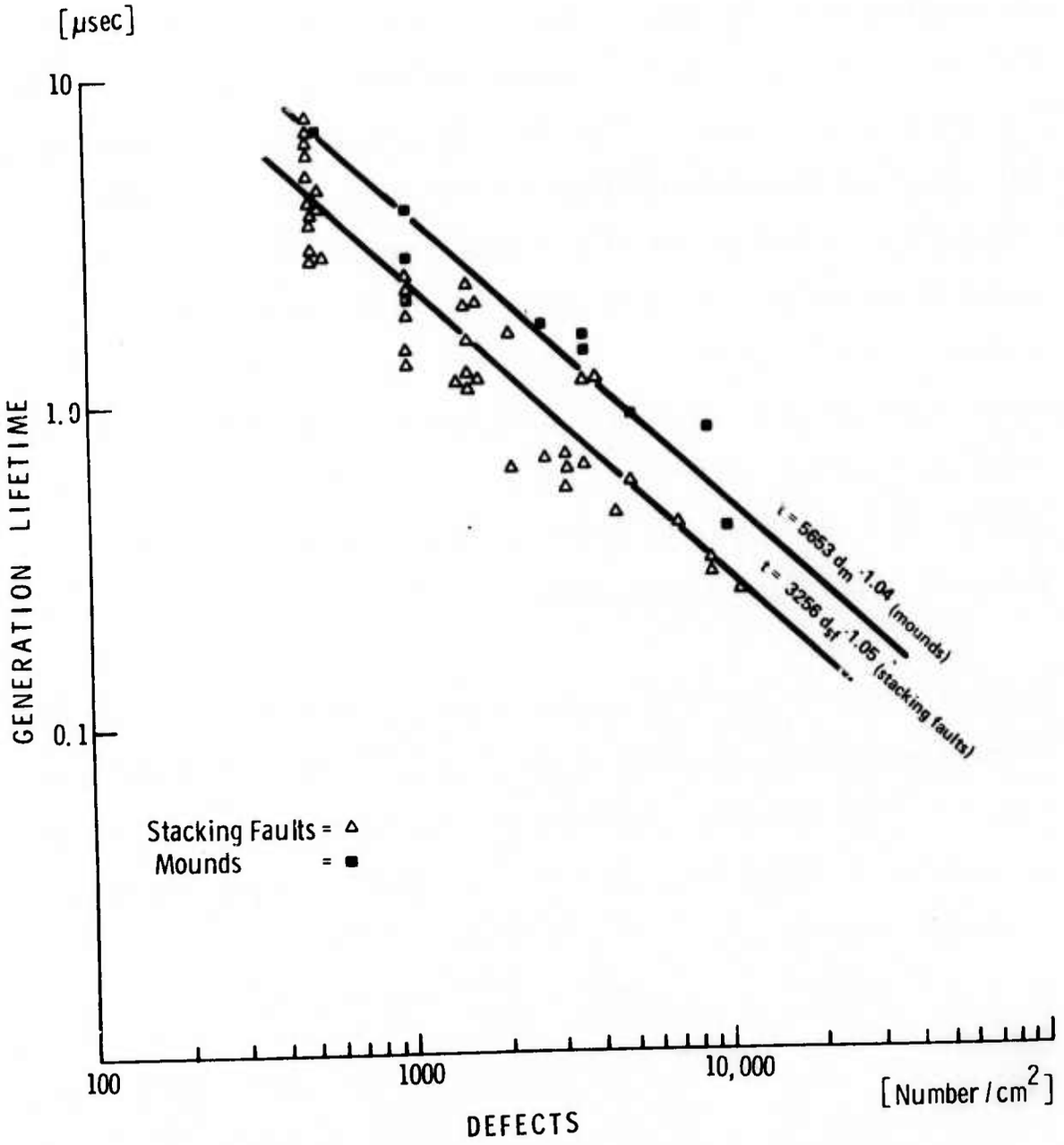


Fig. 24. Lifetime vs. defect dependency.

Equation (2) was obtained from the MOS dots free of defects except mounds. However, some dots from which Eq. (1) was obtained contained mounds (typically one to three per dot) as well as stacking faults. Because of the relatively small contribution of mounds to lifetime reduction, Eq. (1) is not subject to significant error.

The low density of grown-in stacking faults observed in epitaxial samples made it impossible to achieve a reliable estimate of their contribution to lifetime reduction. Their contribution is estimated to be equal to that of mounds or smaller.

A similar correlation for oxidation stacking faults vs. lifetime on substrates was also not possible because the density range covered by the faults on substrates was much too narrow. However, based on the similar crystallographic nature of oxidation-induced stacking faults in substrate and in epitaxial films, one can assume that a similar correlation holds for the lifetime-defect dependency in substrate surfaces. This does not exclude that the electrical "activity" of a stacking fault can vary significantly in different samples. Differences in electrical activity, for instance, due to precipitated impurities along the partial dislocation, are reflected in the constant A of the correlation. This constant, for instance, has the value of 3256 for stacking faults and 5653 for mounds.

7. SUMMARY

The technique of Impact Sound Stressing (ISS) is discussed. ISS is applied (a) to produce damage on silicon surfaces in a controlled manner and (b) to achieve "damage gettering" in silicon.

ISS damage consists of two features: a fine, strongly directional abrasion producing shallow grooves in the silicon surface, and the formation of Hertzian fracture cones. The grooves are bunched together in clusters of 10 to 15 μm^2 area. Fracture cones measure approximately 50 µm along one side. The damage depth of grooves is approximately 0.2 to 0.4 µm and the fracture cones' depth varies from approximately 10 to 20 µm.

Transmission electron microscopy of fracture cones shows that cleavage of silicon at room temperature does not produce dislocations. However, TEM investigations of grooves show dense pile-ups of shear loops and microsplits.

Annealing of ISS damage during oxidation leads to the formation of dislocation networks and oxidation-induced stacking faults. Damage propagation through the crystal volume - from the damaged surface to the undamaged surface - does not occur.

ISS damage introduced on the wafer backside can be used advantageously to monitor generation-lifetime of electrical carriers during semiconductor processing. This is shown for

silicon substrates, for epitaxial silicon films, and for epitaxial silicon films grown on ion-implanted surfaces. ISS can improve lifetime in silicon by several orders of magnitude. Such lifetime improvements on ISS'ed silicon wafers are correlated with a reduction of crystallographic defects. A quantitative relation between lifetime and defect density is given.

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APPENDIX

Computer Program for Lifetime Generation Data Analysis*

by A. Kran

INTRODUCTION

Lifetime histograms as used in Chapter 2 of this report are generated through a computer program developed for rapid and systematic analysis of lifetime generation data. From lifetime generation measurements, entered by terminal into a timeshared APL/SV system, a statistical analysis of the data for each wafer is performed and printed, together with a histogram to show frequency distribution. Wafer data are stored for subsequent print out and summary reports.

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Short Outline of Program

The computer program performs the following three main operations, initiated by execution of these functions:

START - A control function for acquiring the necessary input information for each wafer. It successively executes INPUT, LTIME, STORAGE, FORMAT and HPLOT. Output consists of a data sheet containing a statistical analysis of wafer data, including a histogram.

REPORT - Performs analysis of stored wafer data. From wafer identification number(s) (IDs) input, the program executes FORMAT, LTIME, and HPLOT, printing as output a combined statistical analysis and histogram of wafers specified.

DISPLAY - Formats and prints any number of single wafer data from storage.

These three functions are executed in accordance with the flowchart given in Figs. A,B,C.

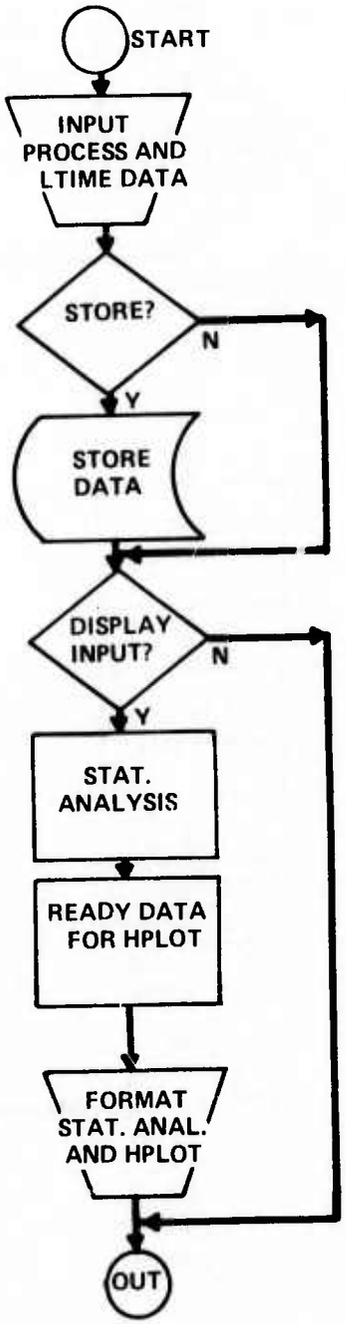

Fig. A. Input program flowchart.

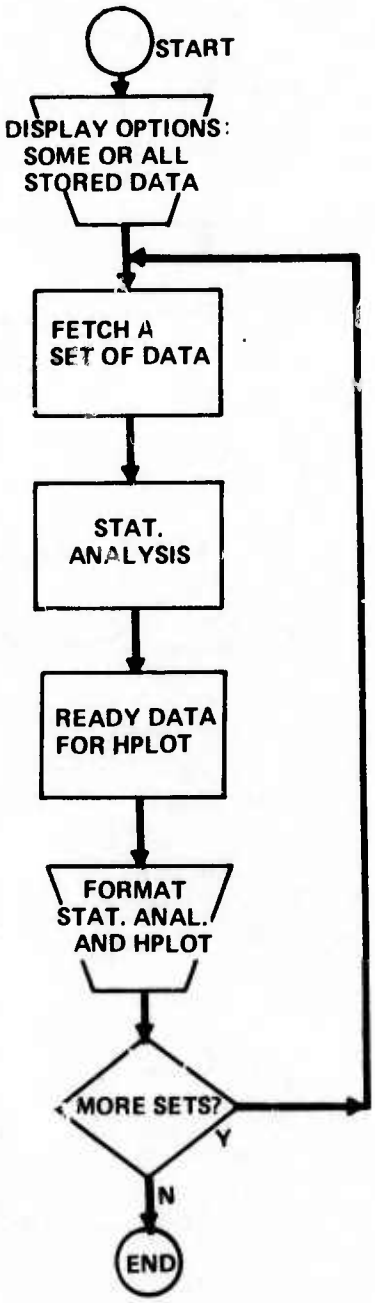

Fig. B. Display program flowchart.

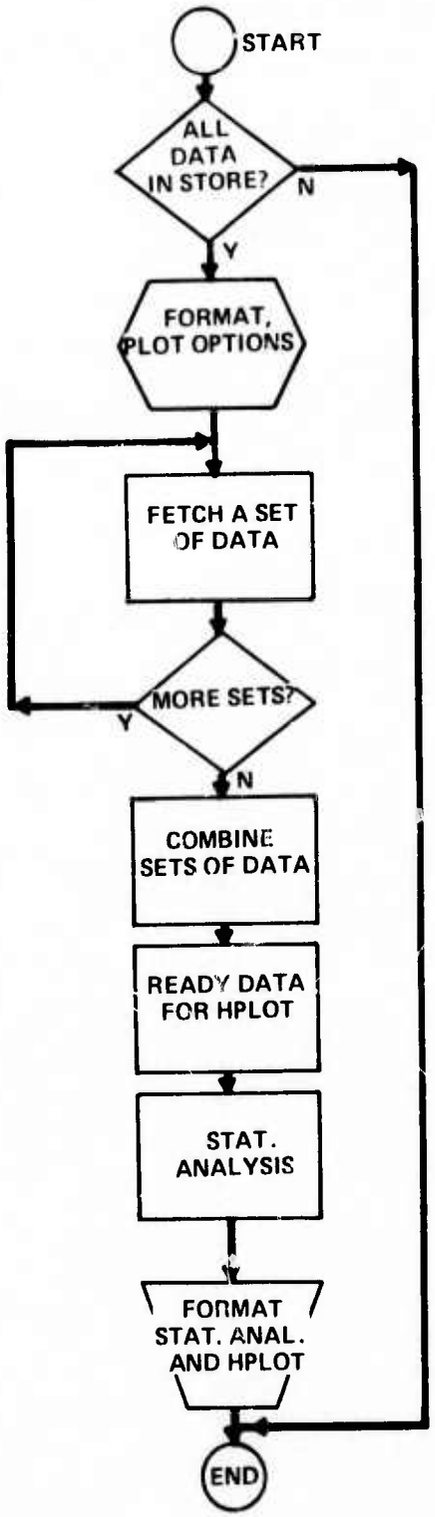

Fig. C. Report program flowchart.

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13. ABSTRACT

The report consists of two chapters. Chapter 1 discusses experimental and theoretical investigations of the growth kinetics of oxidation induced stacking faults. Experimentally it is found that stacking fault growth during wet or dry oxidation follows the equation: $l = A_0 t^{0.77} \cdot \exp \cdot \{- \Delta H_f / kT\}$ where l is the stacking fault length, t is the oxidation time, A_0 is equal to $(1.38 \pm 0.06) .10^9$ for wet oxidation and equal to $(9.5 \pm 0.5) .10^8$ for dry oxidation, and $\Delta H_f = 2.2$ eV the activation energy for fault formation. Theoretically, it is shown that growth of stacking faults can be described through condensation of silicon interstitials at the fault site during oxidation. Condensation of silicon interstitials is controlled through a tensile stress in the silicon surface generated during the formation of the SiO_2 film on the silicon surface. Good agreement between experimental and calculated data for fault length and activation energy is obtained.

Chapter 2 discusses the technique of Impact Sound Stressing (ISS). ISS is applied (a) to produce damage on silicon surfaces in a controlled manner and (b) to achieve "damage gettering" in silicon. ISS damage introduced on the wafer backside is used to monitor generation-lifetime of electrical carriers during semiconductor processing. This is shown for silicon substrates, for epitaxial silicon films, and for epitaxial silicon films grown on ion-implanted surfaces. ISS improves lifetime in silicon by several orders of magnitude. Such lifetime improvements on ISS'ed silicon wafers are correlated with a reduction of crystallographic defects. A quantitative relation between lifetime and defect density is given.

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